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Analysis of Modular Multilevel Converter in HVDC System

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Abstract

Voltage Source Converter (VSC) technology is becoming common in high-voltage direct current (HVDC) transmission systems (especially transmission of offshore wind power). HVDC transmission technology is an important and efficient possibility to transmit high powers over long distances. The vast majority of electric power transmissions were three-phase and this was the common technology which is used widespread. Compared to conventional VSC technology, Modular Multilevel topology instead offers advantages such as higher voltage levels, modular construction, longer maintenance intervals and improved reliability. A multilevel approach has been simulated in MATLAB/SIMULINK throughout this research which actually guarantees a reduction of output harmonics due to sinusoidal output voltages: thus grid filters become negligible, leading to system cost and complexity reduction as well.

Keywords: *Modular Multilevel Converter (MMC), Voltage Source Converter (VSC), Sub Module (SM), Pulse Width Modulation (PWM).*

I. Introduction

Multilevel power conversion was first introduced 20 years ago (B. Chuco *et al* 2011). The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with traditional (two-level) power conversion. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce the dv/dt stresses on the load and reduce the electromagnetic compatibility (EMC) concerns. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses. One clear disadvantage of multilevel power conversion is the larger number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in the multilevel converter and therefore the active semiconductor cost is not appreciably increased when compared with the two level scenarios. However, each active semiconductor added requires associated gate drive circuitry and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices. However, for a complete solution to the voltage-balancing problem, another multilevel converter may be required

II. Methodology

Conventional converters display problems into accomplishing requirements and operation of HVDC transmission (B. Chuco *et al* 2011). The control scheme actually results more complex. Multi-level converter topologies may have advantages and disadvantages during operation or when assembling the converters. So, it is always desired to have such a scheme (U. N. Gnanarathna *et al* 2011). The Multilevel converter system comprises two back-to-back connected MMCs which are herein after referred to as MMC 1 and MMC 2. Each MMC consists arms (considering every phase has lower and upper arms) where each arm includes series-

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connected, nominally identical, half-bridge sub modules (SMs). In this paper 17 level converter has been taken in to consideration. The ac terminal of each MMC is usually connected to a utility grid through a series connected filter, a three-phase transformer (J. Peralta et al 2012). The main circuit diagram of Multi level converter station is given in figure2.

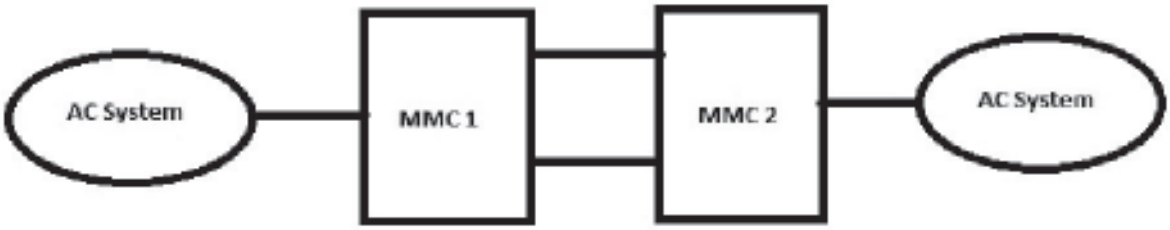

Figure 1: General topology of HVDC System

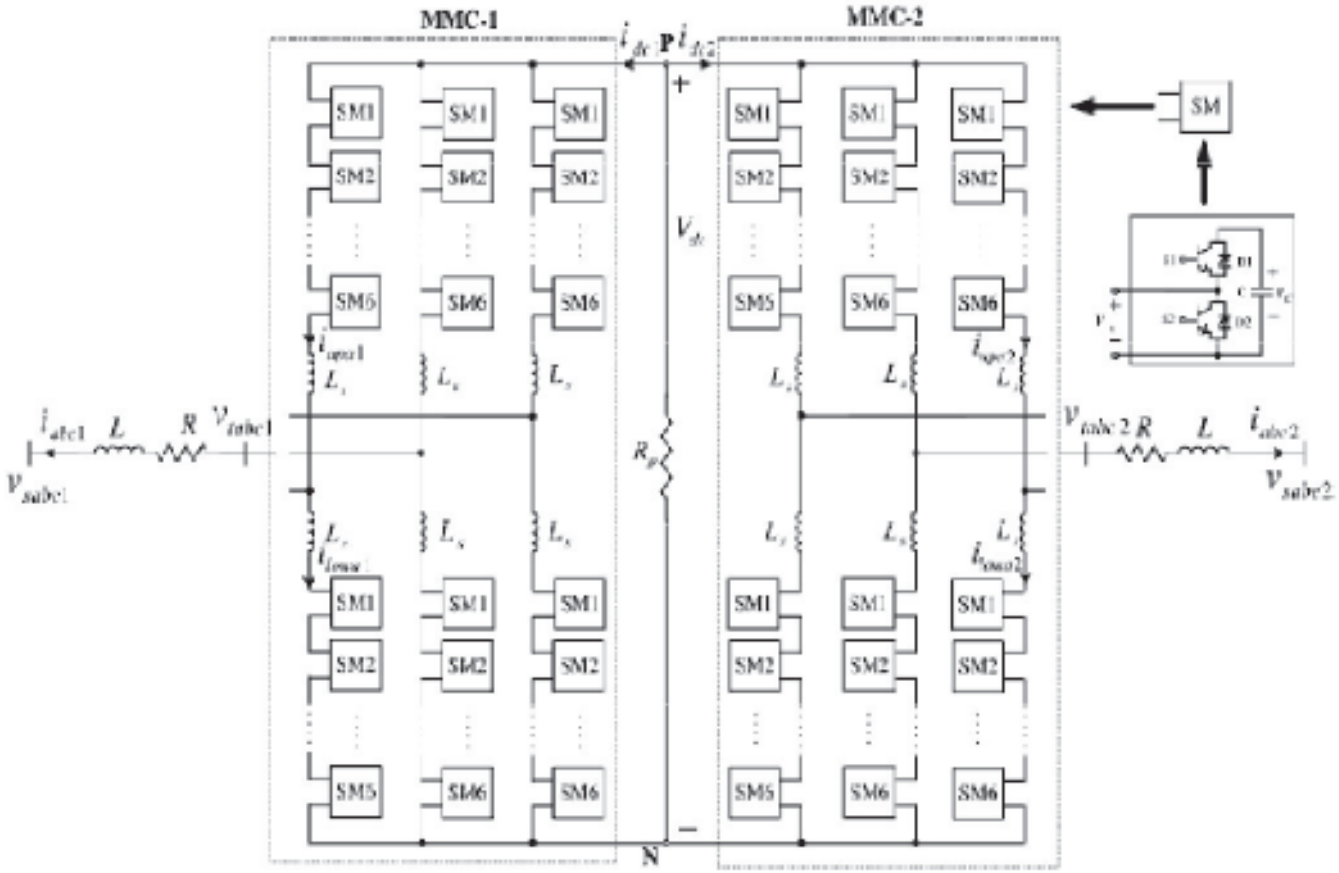

Figure 2: Circuit diagram of multilevel converter station

III. Working Principle

In order to describe the operation of Multi level converter of Figure 2, a functional diagram of single unit MLC is shown in figure 3 where SM (sub

modules) switches are replaced by equivalent two-pole switches (as for example: S_{upa}, S_{upb}, S_{upc} are for upper and S_{lowa}, S_{lowb}, S_{lowc} *are* for lower arms. Every switch has a serial number like 1 to 6 for its identity. If S_{upji} (S_{lowji}) is equal to unity, the output of the *i*th, i= 1,…,6 SM of the upper (lower) arm of phase j= *a, b, c* is equal to the corresponding SM capacitor voltage: otherwise, it is zero. In principle, each MLC arm represents a controllable voltage source which is denoted by (Q Tu *et al* 2011),

$V_{upj}= \sum_{i=1}^{6}(S_{upji}V_{cupji})+ L_s \frac{di_{upj}}{dt}$,

Where j= a,b,c

$V_{lowj}= \sum_{i=1}^{6}(S_{lowji}V_{clowji})+ L_s \frac{di_{lowj}}{dt}$

Here, V_{upj} and V_{lowj} denote the total voltage of the upper and lower arms of corresponding phases. The arm current equations are as below-

$$l_{upj} = \frac{I_j}{2} + \frac{I_{dc}}{3} + I_{zj}$$

$$l_{lowj} = -\frac{I_j}{2} + \frac{I_{dc}}{3} + I_{zj}$$

Here, Izj are the circulating currents which circulate within the three phases of the multilevel converter and $I_{za} + I_{zb} + I_{zc} = 0$.

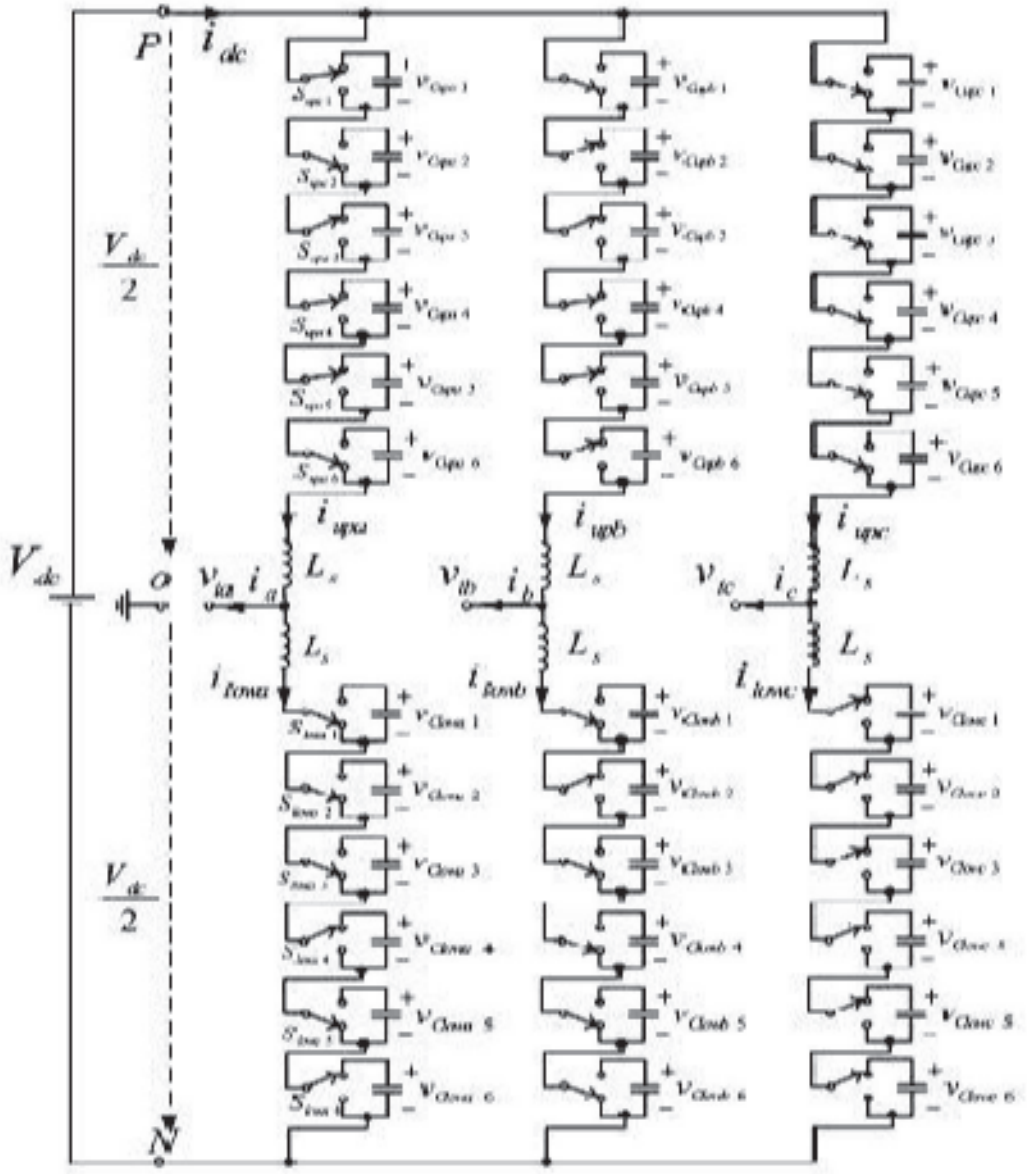

Figure 3: Circuit diagram of single unit multilevel converter

However, they have a significant impact on the rating values of the MMC components and the SM capacitor voltage ripples.
The point '0' is considered as the fictitious dc-side mid-point in Fig 3, the ac-side phase voltages are described by

$$V_{tj} = \frac{V_{dc}}{2} - V_{upj} = -\frac{V_{dc}}{2} + V_{lowj}$$

Based on this and previous arm voltages equations, the switching functions of the SMs in the upper and lower arm of each phase, the arm voltages and, as a result, the ac-side voltages are controlled in discrete steps. The DC voltage of the multilevel converter arms, in each phase is expressed by,

$$V_{dc} = V_{upj} + V_{lowj} = \sum_{i=1}^{6}\left(S_{upji}V_{cupji}\right) + \sum_{i=1}^{6}\left(S_{lowji}V_{clowji}\right) + L_s\frac{di_{upj}}{dt} + L_s\frac{di_{lowj}}{dt}$$

Power equation of multilevel converter is as below-

For DC power,

$$P_{dc} = V_{dc} * I_{dc}$$

For AC power,

$$P_{dc} = P_{ac}$$
$$\text{Or, } P_{ac} = 3V_{dc} * I_{rms}$$

N SMs in the arm, the capacitor energy,

$$W = \frac{C}{2}\sum_{i=1}^{N}(V_{ci})^2$$

A. Functional design of sub modules

Each SM is a simple chopper cell composed of two IGBT switches (S1 and S2) or MOSFET, two anti-parallel diodes (D1 and D2) and a capacitor C. Each phase leg of the converter has two arms, each one constituted by a number N of SMs. Each SM of the MMC consists of a half bridge cell where its output voltage is either equal to its capacitor voltage or zero, depending on the switching states. The switching states and the resultant voltage at the output of each SM are listed in Table 1. There are two complimentary switch pairs (S1 and S2) in each SM.

Table 1: Switching state of sub module

State	S1	S2	Output Voltage
1	On	Off	V_c
2	Off	On	0

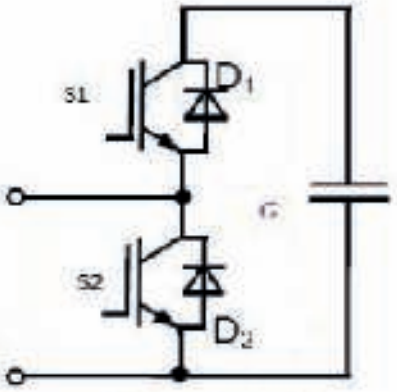

Figure 4: Chopper cell of a sub module

The SM's dc capacitor C stores energy, vital for the operation of HVDC-Multilevel Converter (O Venjakob *et al* 2013). The dc capacitor voltage is kept within a controlled band this important to make possible to generate a desired ac voltage waveform by charging or discharging these capacitors either inserting or by-passing the SMs capacitors. The scheme shown in Fig 4 represents the charging and discharging process of C, during the time interval when the IGBT S1 is conducting this capacitor discharges. During the time when the IGBT S2 is open and the diode in anti-parallel with S1 conducts, the capacitor is charged. When S2 or its anti-parallel diode conducts, the capacitor is bypassed and it is not charged or discharged.
So, it is possible to write-

$$\Delta V_c = \frac{1}{C}\int_{t0}^{t1} i\,dt$$
$$\text{Or, } C = \frac{1}{V_c}\,i\Delta t$$

The voltage variation on the capacitor should be limited to 5% of its rated value or less. The capacitor size can be calculated considering the

worst case, where the Δt is equal to time equivalent to a half cycle (maximum time that capacitor can be inserted). The current through C is defined by $\frac{i_{ac}}{3} + \frac{i_{ac}}{2}$

B. Mode of Operation

The mode of operation is not as difficult as its topology. To understand the operation of multilevel converter we need to concentrate on lower level of converter as for example, one phase of three level converters.

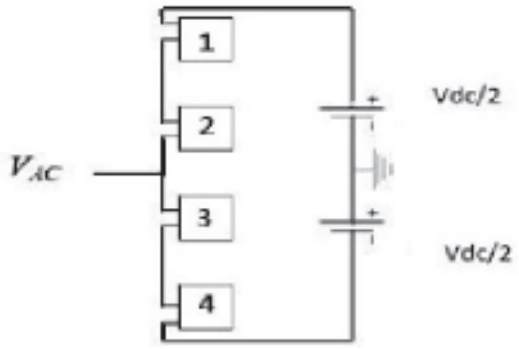

Figure 5: Schematic of one phase of three-level converter

In this case, in order to get the positive output, $+Vdc/2$, the two upper SMs 1 and 2 are bypassed. Accordingly, for the negative output, - Vdc/2, the two lower SMs 3 and 4 are bypassed. The zero state can be obtained through two possible switch configurations. The first one is when the two SMs in the middle of a leg (2 and 3) are bypassed, and the second one is when the end SMs of a leg (1 and 4) is bypassed. It has to be noted that the current flows through the SMS that are not by passed determining the charging or discharging of the capacitors depending on the current direction. Therefore, in order to keep the capacitor voltages balanced, both zero states must be used alternatively. The voltage waveform generated by the three level converters is shown in Figure 6.

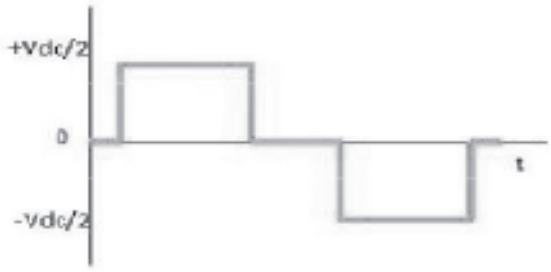

Figure 6: Voltage waveform of a three-Level converter

The principle of operation can be extended to any multi-level configuration as the one represented in Figure 7.

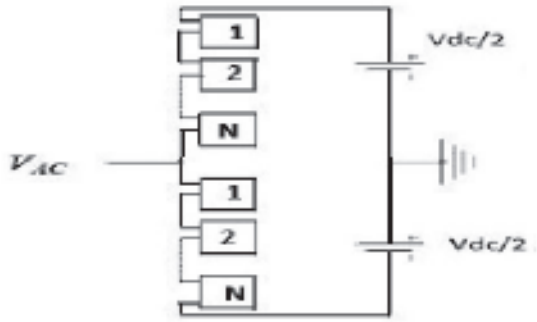

Figure 7: Schematic one phase of Multi level Converter

In this type of converter, the only states that have no redundant configurations are the two states that generate the maximum positive and negative voltages, + Vdc/2 and –Vdc/2. For generating the other levels, in general there are several possible switching configurations that can be selected in order to keep the capacitor voltages balanced. In this multilevel Converter, the switching sequence is controlled so that at each instant only N SMs (half of the 2N SMs of a phase leg) are in the on-state. The SM is the basic element of a MMC topology shown in With N SMs per converter arm it is possible to generate voltage waveform with (2N+1)-levels. As an example, if at a given instant in the upper arm SMs from 2 to N are in the on-state, in the lower arm only one SM will be in on-state. It is clear that there are several possible switching configurations. Equal voltage sharing among the capacitor of each arm can be achieved by a selection algorithm of inserted or bypassed SMs during each sampling period of

the control system. A typical voltage waveform of a multi-level converter is shown in Figure 8.

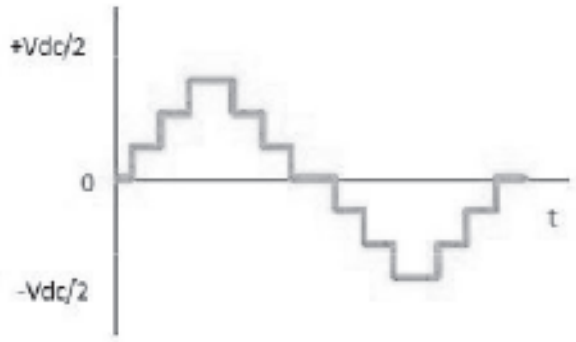

Figure 8: Voltage waveform of a multilevel Converter

C. Control scheme (PWM Method)

To control and balance the dc capacitor voltage, the current of the converter arms and the capacitor voltages are considered (measured) to choose the operation mode of the sub modules (SMs) (H Sadat *et al* 2013). Similar to multilevel topologies, the capacitor voltages of the individual SMs must be monitored and kept equal. The PWM (Pulse Width Modulation) strategy determines the number of SMs that should be on in the upper and lower arms of the converter. For a specified number of SMs in the upper and lower arms, there are several switching combinations. Capacitor voltage values and also the direction of the arm currents are used to select SMs in the upper (lower) arm and to determine which SMs should be switched on (T. L Maguire *et al* 2013).

To synthesize a N-level waveform at the ac-side of the converter, a PD-SPWM strategy is usually applied (M. Saeedifard *et al* 2010). The PD technique requires N-1 in-phase carrier waveforms displaced symmetrically with respect to the zero-axis. By comparing a sinusoidal reference waveform with the N-1 carrier waveforms desired PWM modulation control scheme can be achieved.

IV. Simulation Results

MMC topology of 17 levels has been developed in MATLAB/ SIMULINK throughout the research. A demo three phase AC system has been considered and Phase Locked Loop (PLL) has also been utilized in the model. Voltage measurement scheme has been used, so that the output waveform can be observed through the scope. The harmonic result can be obtained by FFT analysis.

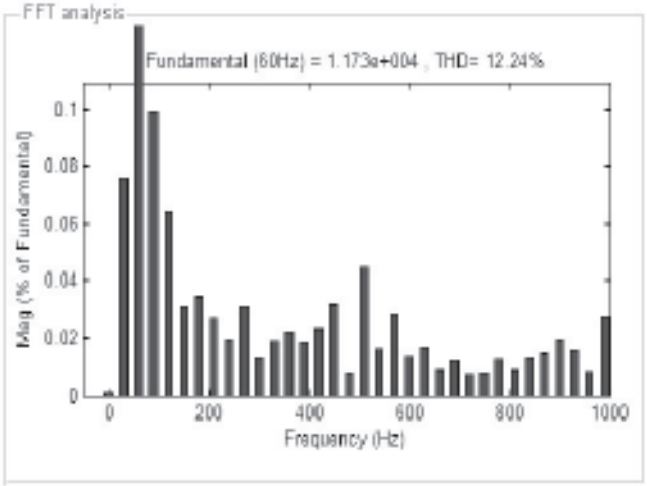

Figure 11: FFT analysis

We can see from the figure that the total harmonic distortion has been of almost 12% which is under considerable range.

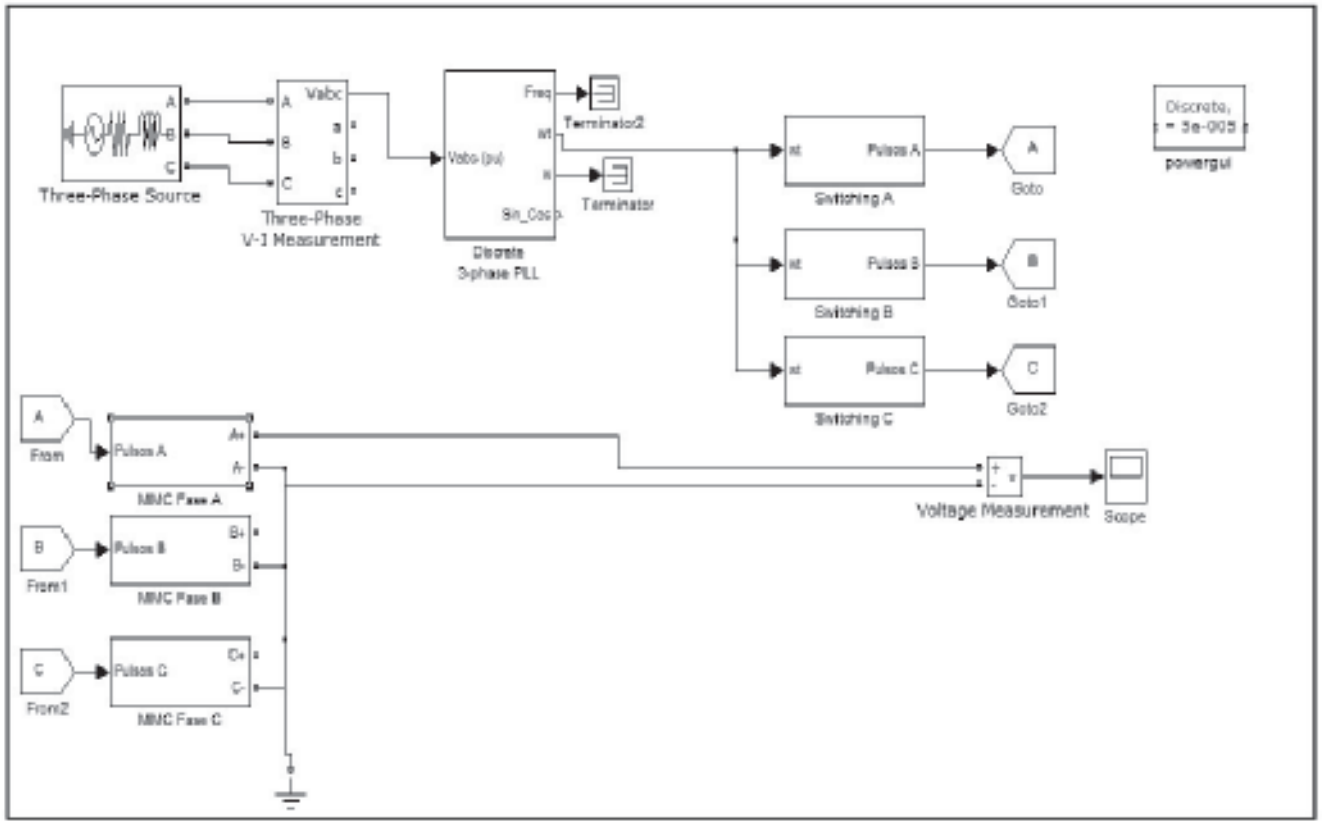

Figure 11: SIMULINK Model for a 17 levels MMC topology

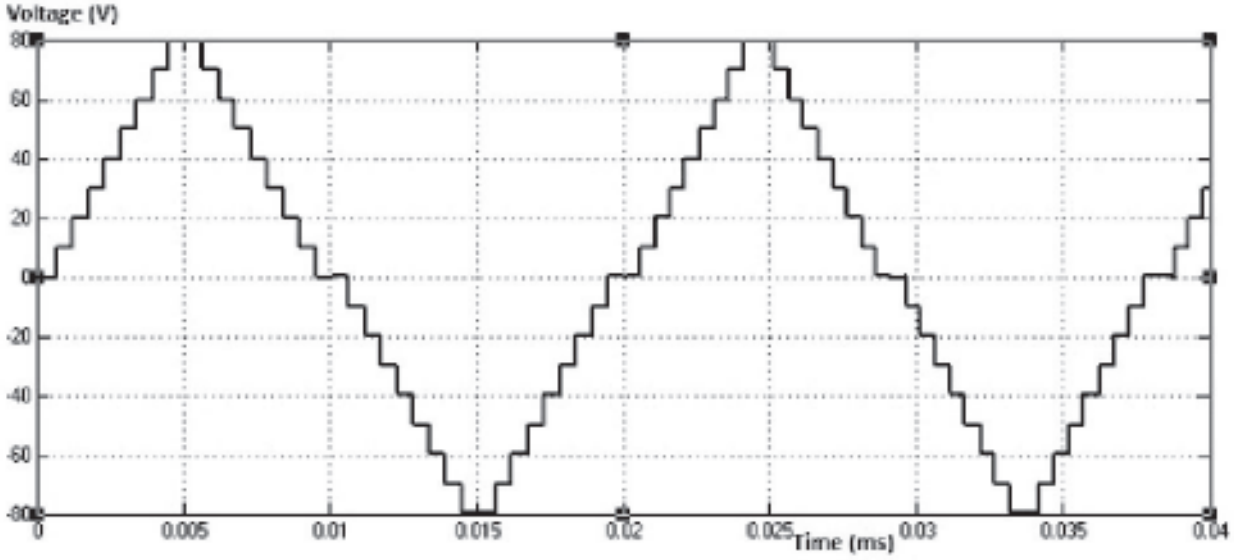

Figure 12: Output Voltage wave-shape

The Phase Locked Loop (PLL) system in SIMULINK model has been used to synchronize on a set of variable frequency, three-phase sinusoidal signals. Initial phase has been given 0 and the allocated frequency has also be given in 50 Hz. The regulator gain is given 60 and 1400 respectively for K_p and K_i. Pulse generator has been used to configure the desired switching

condition. The output is a 17 levels wave-shape which is observed through the scope of voltage measurement scheme.

V. Conclusion

In this research, a back to back VSC HVDC Transmission system based on a 17 level multilevel converter control scheme has been highlighted. Only the output of MMC scheme is analyzed in this report. The scheme can be broadened to numerous levels, concept will be the same but control will be much more complex and so many harmonics will be included as well for the continuous switching of IGBTs (M. Matar *et al* 2013). To ensure a healthy operation of multilevel converter, we need to consider also IGBT power losses which consist of conduction losses and switching losses (N. Flourentzou *et al* 2009). Although there are complexities, but still multilevel converter is considered as an efficient tool for HVDC transmission network in modern days.

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