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A Review of the Fabrication Process of the Pocket Implanted MOSFET Structure

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Abstract
The dimensions of the various types of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device structures are being shrunk continuously to accommodate more transistors inside a single chip. However, these shrinking entail several impacts on the device performance degradation and hence it has become cumbersome to operate the device properly at its various biasing conditions. To obtain the best performance from the shorter device, the modified device structure is being proposed or developed by the device design engineers. One such effort is to have the additional dopant atoms laterally at the channel region's drain and/or source sides through the ion implantation process. This is known as pocket implantation and the new device structure thus obtained is called pocket implanted MOSFET. Due to this extra doping, the threshold voltage is increased rather than decreased as the channel length is reduced. This new effect is termed the Reverse Short Channel Effect or in short RSCE. However, the new device structure requires new fabrication processes. Therefore, in this paper, the formation processes of the pocket structure have been described in detail by studying the various literature. To fabricate the pocket implanted Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure, we require several fabrication steps, like, Chemical Vapor Deposition (CVD), Ion Implantation, Electron Beam Lithography (EBL), Rapid Thermal Annealing (RTA), Reactive Ion Etching (RIE), etc. All these steps are described herein brief so that a clear picture can be obtained about it The knowledge of these steps can be utilized to derive the various operational parameters, such as surface potential, threshold voltage incorporating bias and temperature effects, effective mobility model, subthreshold drain current, drain current flicker noise, etc. of the pocket implanted n-MOSFET device as well as their modeling and characterization.

Keywords: Fabrication Process, Ion Implantation, Lateral Profile, Pocket Implanted MOSFET.

I. Introduction

Complementary Metal Oxide Semiconductor (CMOS) device dimensions are continuously being shrinking to enhance the circuit speed and density and this has become possible due to the nonstop progress of the semiconductor device process technology (M. A. Riyadi *et al.*, 2010). This reduction of the channel length of MOSFET reduces the threshold voltage. The impact of threshold voltage reduction, with the channel length downscaling, is impeding the future MOS device design and modeling in the nano-scale regime (B. Yu *et al*, 1997). The minimum channel length, L_{min}, which can be recognized, is mainly ascertained by the threshold voltage decrement, which is also identified as the Short Channel Effect (SCE). To combat these Short Channel Effects, various techniques have been introduced. Pocket implants are commonly used to combat short channel effects (M. H. Bhuyan *et al.*, 2006; M. H. Bhuyan, 2011). The threshold voltage decrease can be stopped or even can be increased with the channel length decrease by enhancing the doping concentration nearby the drain and/or source regions in the channel. Consequently, this causes the subthreshold leakage current decline. However, the driving capability of the device is enriched. The phenomenon of threshold voltage increment with the channel length decrement is popularly recognized as the Reverse Short Channel Effect (RSCE) (M. H. Bhuyan, 2011; M. H. Bhuyan and Q. D. M. Khosru, 2010; M. H. Bhuyan *et al.*, 2006). This behavior is opposite of what is expected from the Short Channel Effect.

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There are many causes to produce reverse short channel effects in the MOSFET. One of the sources of this effect, the threshold voltage can rise right after the channel length greater than the smallest channel length of that technology node. Another birthplace of RSCE is the channel doping concentration build-up due to oxidation-enhanced-diffusion (M. Orlowski *et al*., 1987), implant-damage-enhanced diffusion (M. Nishida and H. Onodera, 1981) which is very difficult to control, the electrical deactivation of arsenic or boron penetration from poly-gate and oxide (R. H. Dennard *et al*., 1974). However, there may have some other reasons, for example, annealing (D. J. Frank, 1997) and Salicide (B. Davari *et al*., 1995) within front end methods that may impact on the RSCE. The local higher doping volume density is created close to the source/drain junctions in the channel through the lateral channel engineering, e.g., halo (P. K. Chatterjee *et al*., 1980) or pocket implants (G. Meindl *et al*., 1981). These two terms carry almost the same meaning. However, a halo connotes a pocket that is profound than the drain side. There are two types of implants- one is called symmetrical (G. Meindl *et al*., 1981; J. Baccarani *et al*., 1984) and the other is called asymmetrical (T. N. Buti *et al*, 1989) concerning the source and drain regions of the channel.

In the literature, a few circuit applications were reported. One example that has been found was a 256-Mbit DRAM (A. Chatterjee *et al*, 1994) and another such example was a mixed-signal processor (H. Chen *et al*, 1994). Besides, in a 0.1 μm n-channel and buried p-channel MOSFET using Large-Angle-Tilt-Implanted (LATI) pocket could show an excellent performance improvement over SCE (J. Baccarani *et al*., 1984). Therefore, we can say that the pocket implantation knowledge is a very effective technology to alter the SCE performance of deep-submicron as well as nano-scale regime MOSFETs.

In this paper, we will first discuss the two important processes- diffusion and ion implantation techniques as well as other related techniques that are necessary to form the pocket implanted MOSFET structure. Then the structure and formation processes of a pocket implanted MOSFET structure. Then we will suggest the characterization of the pocket doping profile.

II. Fabrication Processes

The critical physical boundary of MOS transistor downscaling is supposed to be the space of atoms in the Si lattice structure in the vicinity of 0.3 nm (H. Iwai *et al*., 2006). As such, after this limit, further downscaling of the MOS transistor would be impractical and cumbersome. Therefore, the researchers are investigating enthusiastically for new materials and novel device structures (M. H. Bhuyan, 2017; M. H. Bhuyan, 2018; M. H. Bhuyan, 2019). In this section different conventional fabrication processes, such as diffusion, ion implantation, chemical vapor deposition, etching, thermal annealing, etc. will be described. However, fabrication processes of physical MOS transistor structure are being implemented using Athena simulator while the electrical characterization of such devices is being simulated by ATLAS simulator (M. N. Sachdeva and M. Vashishath, 2016).

A. Diffusion Process

The diffusion process is an elementary property of any material that is defined as the motion of a particle, like an atom, molecule electron, hole, or ion, from one material to another material. However, the diffusion process initiates when the concentration of the particle differs in the two materials. The particle flows from the higher concentration material into the material with the lower concentration. In semiconductor fabrication, high-temperature diffusion is the mechanism used to move a dopant through the Si crystal lattice. Diffusion can occur as gas, liquid, or solid-state. When a high concentration of dopant material is introduced into a wafer it starts to diffuse into the whole crystal lattice (J. R. Brews *et al*., 1980).

Thermal diffusion of a solid-state Si requires three steps: pre-deposition, drive-in, and activation. During pre-deposition, wafers are loaded into a high-temperature diffusion furnace and a quantity of dopant atoms is transformed from the source cabinet to the diffusion furnace. The furnace temperature setting is typically 800^0C to 1100^0C from 10 to 30 minutes. Then the dopants are given into the thin layer of the wafer by maintaining a constant surface dopant concentration. After that, a thin oxide layer, known as cap oxide, is grown on the surface to inhibit dopant atoms from being diffused out of the Silicon. The concentration of dopants is the

highest at the surface and reduces when moving away from the surface, forming a gradient or slope that creates the dopant profile. Fick's law, first postulated in 1855, mathematically describes the diffusion process. This law describes that the number of particles per unit area per unit time, known as diffusion flux, is directly proportional to the concentration gradient, given by equation (1).

$$F = -D\nabla c \quad (1)$$

,where c is the concentration of the diffusing particles (number per unit volume), F is the diffusion flux (number per unit area per unit time), and D is the diffusion constant (cm^2/s). For a one-dimensional problem, Fick's law can be expressed by equation (2) along the x-axis.

$$F = -D\,dc/dx \quad (2)$$

Fick's law is used to predict the dopant concentrations at some distance, x, from the surface (E. Quek, 2005).

In the high temperature (1000^0C to 1250^0C) drive-in process, the deposited dopant atoms travel through the Si crystal to the desired junction depth in the wafer. However, the wafer surface oxidizes in the high-temperature environment and dopant atoms redistribute in the crystal.

Finally, in the activation step, the temperature of the furnace is raised slightly greater to enable the dopant atoms to make a bond with the Si atoms in its crystal structure. This action activates the dopant atoms, which changes the conductivity of the doped Si material.

Each dopant has a particular diffusivity in Si, which represents the rate or speed that the dopant moves in the wafer. The higher value of diffusivity means that the dopant inside the crystal will move faster. However, the diffusivity increases with the rise of crystal temperature, which is reflected in the diffusion coefficient, D of the dopant to be diffused in the crystal. Thus dopants in the wafer transport through two different mechanisms, viz. interstitial and substitutional as shown in Fig. 1.

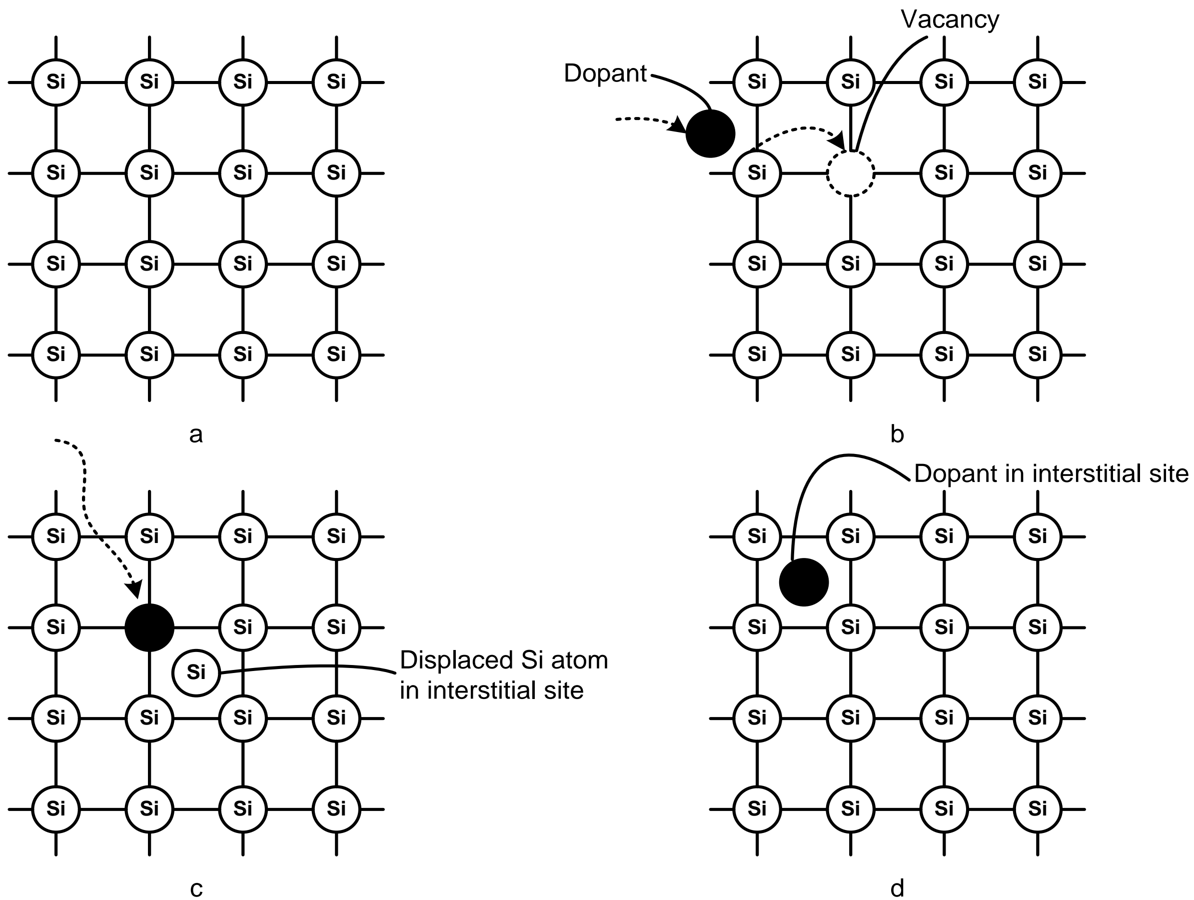


Figure 1: Dopant diffusion in Si, (a) Si lattice structure, (b) Substitutional diffusion, (c) mechanical interstitial displacement, (d) interstitial diffusion

Dopants with high diffusivities, such as gold, copper, and nickel, use primarily interstitial movement to move between the interstitial spaces between regular crystal sites of the Si lattice. Slower moving dopants, such as, arsenic and phosphorous that are common in semiconductor doping, typically use substitutional movement where atoms fill empty crystal positions in the lattice. Dopants are useful to form semiconductor Si only if they are activated dopants, i.e. if they are part of the Si lattice structure. An activated dopant can act as a donor or acceptor of electrons and is an n-type or p-type dopant concerning Si. If the dopant occupies interstitial space, then it is not activated and is ineffective as a dopant. Thermal energy moves dopants into the regular crystal sites, a process known as crystal activation.

At a given temperature, there is a limit to how much dopant can be absorbed by the Si. This is referred to as the solid solubility limit and it is given for some materials in Table 1.

Table 1: Solid solubility limits in Si at 1100^0C

Dopant	Solubility limit (atoms/cm^2)
Arsenic (As)	1.7×10^{21}
Phosphorous (P)	1.1×10^{21}
Boron (B)	2.2×10^{20}
Antimony (Sb)	5.0×10^{19}
Aluminium (Al)	1.8×10^{19}

The diffusion mask is either SiO_2 or Si_3N_4 since a photoresist mask could not withstand the high-temperature process. When atoms diffuse into the wafer, they move in all directions- down into the SI, laterally, and back out of the wafer. Lateral diffusion occurs when dopant atoms transit along a path of the wafer surface region. Typically, lateral diffusion is 75 to 85% of the vertical junction depth during a thermal diffusion process. Lateral diffusion is undesirable in advanced MOS circuits because it can cause a reduction in the channel length, affecting device density and performance.

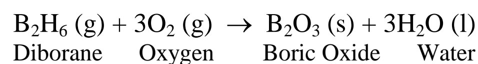
The objective of the diffusion process is to bring the diffusing impurity in contact with a wafer and maintain the specified time and temperature for diffusion to occur. Diffusion takes place in a high-temperature diffusion furnace where all three steps occur. Diffusion should produce reproducible results from run-to-run and wafer-to-wafer. The eight steps that are essential to achieve diffusion processes properly in the wafer production process are as follows:

1. Start the qualification test to meet the criteria of production quality.
2. Validate the features of the wafer utilizing a lot of control schemes.
3. Transfer the procedure recipe with the preferred diffusion parameters.
4. Set up the diffusion process furnace with a temperature profile.
5. Clean the wafers and immerse them in HF acid to eliminate the inherent oxide.
6. Implement pre-deposition: load wafers into the deposition furnace and diffuse the dopant into the wafer.
7. Perform the drive-in: raise the temperature of the furnace to the drive-in and stimulate the dopant bonds, then unload the wafers.
8. Measure, evaluate, and record the junction depth and sheet resistivity.

Dopants are supplied as a gaseous or liquid source in the form of a compound. A few frequently used dopants' names with their source's formulas are shown in Table 2.

A liquid source has a carrier gas (e.g., N_2) bubbled through it and is delivered to the furnace tube as a vapor. Oxygen is also supplied for the dopant source to react and form oxides. Using boron as an example, the boric oxide undergoes a second reaction with Si to form a boron-rich SiO_2 layer on the top of the wafer. This layer serves as the local source of boron for the pre-deposition step. The following two reaction equations illustrate how the diborane source is converted into a boron dopant.

1st reaction:



2nd reaction:

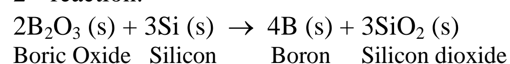


Table 2: Typical dopant sources for diffusion

Dopant	Formula of Source	Chemical Name
Arsenic (As)	AsH_3	Arsine (gas)
Phosphorous (P)	PH_3	Phosphine (gas)
Phosphorous (P)	$POCl_3$	Phosphorus oxychloride (liquid)
Boron (B)	B_2H_6	Diborane (gas)
Boron (B)	BF_3	Boron tri-fluoride (gas)
Boron (B)	BBr_3	Boron tri-bromide (liquid)
Antimony (Sb)	$SbCl_5$	Antimony pentachloride (solid)

B. Ion Implantation Process

Ion implantation is a method to bring together controlled amounts of dopants into the Si substrate to change its electronic properties. It is a physical process; there are no chemical reactions like the diffusion process. The key area of the ion implantation process is in the doping process of semiconductor ingredients (J. R. Brews *et al.*, 1980).

Ion implant processing is done in one of the most complex semiconductor processing tools, called the ion implanter as shown in Fig. 2. The implanter has an ion source component that creates positive-charged dopant ions from the source material. The ions are extracted and then separated in a mass analyzer to form a beam of the desired dopant ions. The number of ions in the beam is correlated to the preferred dopant concentration to be added to the wafer. The beam of ions is augmented in an electric field to achieve a high velocity (of the order of 10^7 cm/sec) (Y. Taur *et al.*, 1985). Because of the high velocity, the ions have kinetic energy that is used to implant the dopants into the Si crystal lattice structure of the target wafer. The beam scans the wafer to provide uniform doping across the wafer surface. After the ion implantation technique, thermal anneal is applied to initiate the dopant ions in the crystal structure. All implanter processing is completed in a high vacuum.

There are two major goals for nanoscale doping requirements:

- To introduce a uniform, controlled amount of a specific dopant into the wafer.
- To place the dopants at the desired depth.
- To generate a precise sharing of dopants at the wafer surface.

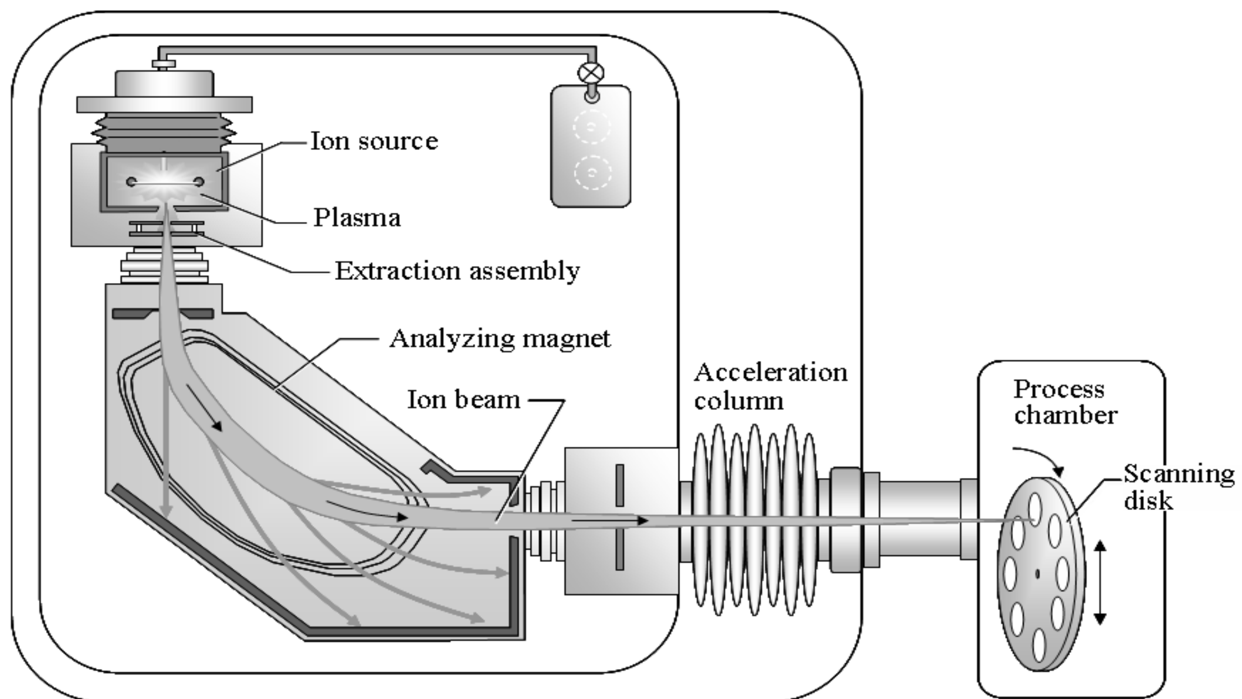


Figure 2: General schematic of an ion implanter

The major benefits of the ion implantation technique are as follows:

- Defined dopant concentration
- Uniform dopant atoms sharing
- Control of penetration depth of dopants
- Pure ion beam creation
- Low processing temperature
- Implanting dopant atoms through films
- The inexhaustible solid solubility of dopant

The major detriments of ion implantation are as follows:

- The damage is done to the crystal structure when the energetic dopant ions bombard the Si host atoms
- The complexity of implanter equipment

However, the last drawback is offset by the implanter's capability for dose and depth control and overall process flexibility. The two most noteworthy ion implantation performance features are the ion dose and ion range.

- **Ion Dose:** It is defined as the number of entrenched ions per unit surface area of the wafer. It is measured in atoms/cm^2 or ions/cm^2. The implanted ion dose, Q is calculated by the ion dose equation (1).

$$Q = \frac{It}{qnA} \quad (1),$$

where Q is the dose, I is beam current, t is the time, q is the charge of the electron, n is the number of charge per ion and A is the surface area of the wafer where ions are to be implanted.

- **Ion Range:** It is the total length an ion moves in the wafer for the entire duration of the ion implantation process. To characterize range, it is necessary to understand energy. When the ions are accelerated due to electric potential difference to a high velocity, they gain energy. The ion energy is kinetic (E_k) due to its motion, and it typically is expressed in units of joules. However, for ion implantation, the energy is usually specified in terms of the number of the electronic charge times the difference in potential or electron volts (eV). The equation that describes this energy is given by equation (2).

$$E_k = nV \quad (2),$$

where E_k is energy in eV, n is the charge state of the ion and V is voltage difference in volts. Higher implantation energy means the dopant atoms will have an increased range and penetrate deeper into the wafer. Energy is important in implanters because of the need to control the range and thus the junction depth of the dopants. High energy implant is used in applications, such as deep retrograde wells and retrograde triple wells as shown in Table 3. A retrograde well has higher doping concentrations deeper in the well than at the surface. Ultra-low energy implanters have energies down to about 200 eV to enable doping at very shallow depths for source/drain applications (P. M. Rousseau *et al*., 1997).

Table 3: Classes of implanters

Implanter System Class	Description and Application
Low/Medium Current	▪ Highly pure beam currents < 10 mA ▪ Beam energy is usually < 180 KeV ▪ Most often the wafer remains immobile and the ion beam is scanned ▪ Specialized applications of punch through stops
High Current	▪ Generate beam currents > 10 mA and up to 25 mA for high dose implants ▪ Beam energy is usually <120 KeV ▪ Most often the ion beam remains immobile and the wafer scans ▪ Ultra-low energy beams (< 4 KeV down to 200 eV) for implanting ultra-shallow source/drain junctions
High Energy	▪ Beam energy exceeds 200 KeV to several MeV ▪ Place dopants beneath a trench or thick oxide layer ▪ Able to form retrograde wells and buried layers
Oxygen Ion Implanters	▪ Class of high current systems used to implant oxygen in SOI applications

There is a projected range, R_p, which is how far the implanted ions travel into the wafer, depending on the ion mass and ion energy, the target mass, and the beam direction concerning the wafer crystal assembly as presented in Fig. 3 (C. Subramanian *et al*., 1995). At the same time, not all ions come to stop simply at the projected range, some stop at a shorter distance and others at a

greater distance. Ions will also move in a lateral direction. Combining all these ion movements produces a distribution of distances traveled by the dopant atoms implanted in the wafer, referred to as straggle, or ΔR_p. The projected range indicates how shallow or deep the junction depth can be formed, whereas the straggle represents the spread of the implanted species around R_n. As the implant energy of dopant atoms increases, the projected range increases but the peak concentration of dopants decreases because the range straggling increases.

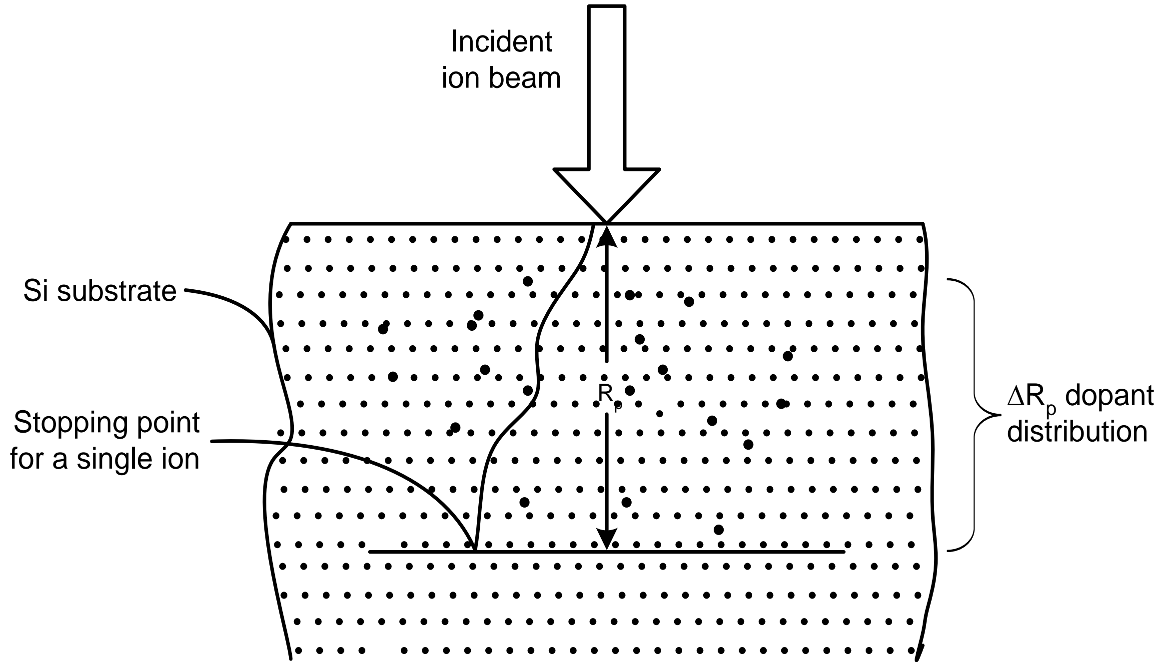


Figure 3: Range and projected range of dopant ion

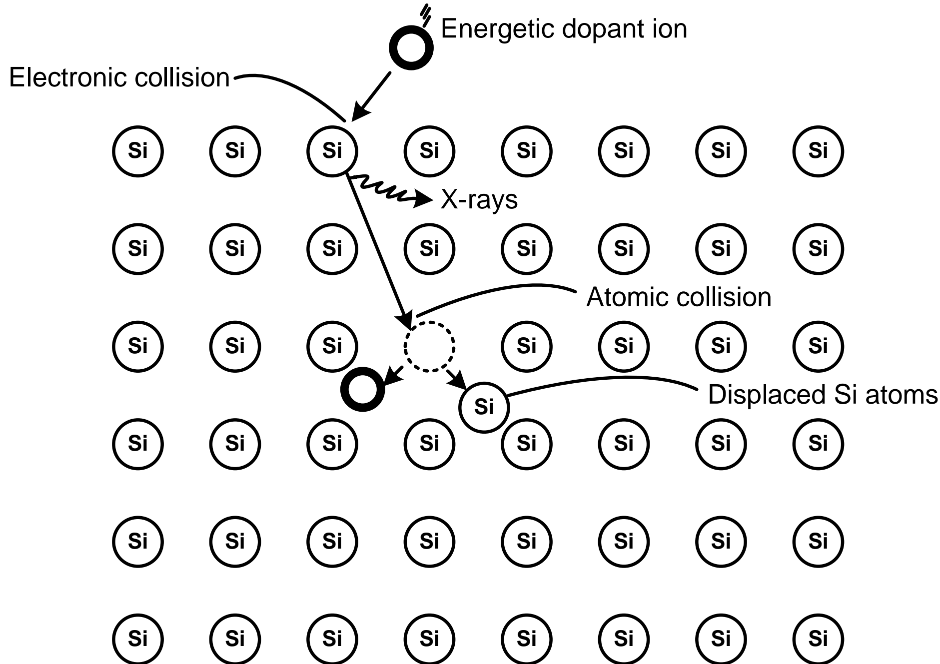


Figure 4: Energy loss of an implanted dopant atom

The implanted ions will travel some depth into the target wafer before they are brought to rest by energy loss due to collisions with Si atoms as shown in Fig. 4. The two primary loss mechanisms are electronic stopping and nuclear stopping (L. D. Yau, 1974). Electronic stopping of dopant atoms is caused by interactions with the target electrons, similar to stopping a projectile in a thick medium. The nuclear stopping of implanted ions is caused by collisions between two hard spheres. Depending on the ion mass and energy, an implanted atom can displace as many as 10^4 Si atoms by nuclear collisions before coming to rest (Q. Wensheng, *et al*., 2003).

The dopant atoms to be implanted must remain existent in the ion beam as a charged particle or ion. Because of their electrical charge, ions can be controlled and accelerated with electric and magnetic fields. Ions for implantation are generated in an ion source. A positive ion is formed from a dopant gas some or by vaporizing a solid. Typically B^+, P^+, $As^{+,}$ and Sb^+ are produced by the ionization of atoms or molecules. The most common feed material for a source of dopant atoms is a gas, such as B_2H_6, BF_3, $PH_{3,}$ and AsH_3. Ions are generated in the ion source by bombarding the feed gas atoms with electrons. Electrons are often produced by a simple and robust hot tungsten filament source. The Freeman ion source is one of the most common electron sources (C. Subramanian *et al*., 1995). The bombardment of electrons breaks up the feed gas molecule into different ion species. BF_3 is often used as a feed gas and in that case generated ion species are B^+, $B_{10}{}^+$, $B_{11}{}^+$, BF^+, $BF_2{}^+$, $F^{+,}$ and $F_2{}^+$. The B^+ ion is the atom desired to be implanted into the wafer and will be selected when the beam passes through the analyzer magnet.

The traditional implanter extraction system collects all the positive ions created inside the ion source and forms them into a beam. The ions are extracted through a slit in the ion source. These ions contain many different ion species and travel at a relatively high speed due to the acceleration provided by the extraction voltage. A magnetic ion analyzer separates the desired dopant ion from the main body of ion species by adjusting the magnetic field strength and the desirable dopant ion passes through a slit at the end of the analyzer while all other ions strike the walls of the analyzing magnet. To achieve additional ion acceleration beyond the analyzer magnet, positive ions are accelerated in an electric field inside an acceleration column. The higher is the total voltage difference in the column, the higher is the velocity of the ions and, therefore, is the energy. Higher beam energy means the dopant ions are implanted deeper into the wafer, while lower beam energy is used for ultra-shallow implants.

The dose versus energy map highlights the importance of energy (range) and dose (concentration) for ion implantation (J. R. Brews *et al*., 1980). Beam energy defines the projected range that the ions are implanted in the wafer surface and varies from high energy (>200 KeV and into multiple MeV) to low energy (<120 KeV and down to 200 eV). The dose is directly associated with the concentration of dopants in the wafer and is represented by the beam currents, or the number of ions in the beam ranging from low, medium to high current (>15 mA). Implanters are often classified according to their maximum operating beam current and acceleration energy.

There is an additional beam focusing that takes place in the post accelerator component of the acceleration column. It typically uses a quadrupole lens focusing based on four cylindrical poles in a two-lens system, employing electrostatic or magnetic repulsion to form the ion beam into a focused circular beam.

C. Deposition Techniques

Microchip fabrication is a planar process comprising many different film layers on the surface of the wafer. The deposition is a procedure that places the film layers on the wafer. While the doped regions and p-n junctions encompass the electrically active modules in a circuit, it precedes several other layers of semiconductors, dielectrics, and conductors to complete the device or circuit. Many layers are deposited on the wafer by Chemical Vapor Deposition (CVD) techniques. The CVD process is defined as the course of action to deposit a solid film on the wafer surface via a chemical reaction of a gas combination. The wafer surface or its neighborhood is heated so that it can deliver extra energy into the system to initiate the chemical reactions. The crucial features of CVD techniques are:

1. A chemical reaction must be required here. It may be either through any chemical reaction or by thermal decomposition.
2. All the required materials for the thin film deposition must be delivered from an external chemical source.
3. The reactants in a CVD method must begin in the vapor phase stage (as a gas).

The Chemical Vapor Deposition technique is a method that uses the chemical reactions that occur when chemical compounds are assorted and then chemical reactions take place in a suitable deposition chamber, called a reactor. After that, the atoms and/or molecules start to deposit on the wafer surface and gradually they form the film. The different types of CVD processes and their principal characteristics are shown in Table 4 (C. Y. Lu and J. M. Sung, 1989).

Table 4: Types of CVD reactors and principal characteristics

Process	Advantages	Disadvantages	Applications
APCVD (Atmospheric Pressure CVD)	The simple reactor, fast deposition, low temperature.	Poor step coverage, particle contamination, and low throughput.	Low-temperature oxides (both doped and undoped).
LPCVD (Low-Pressure CVD)	Excellent purity and uniformity, conformal step coverage, large wafer capacity.	High temperature, low deposition rate, more maintenance-intensive and requires a vacuum system.	High-temperature oxides (both doped and undoped), Si_3N_4, polysilicon, W, WSi_2.
Plasma Assisted CVD: ▪ Plasma Enhanced CVD (PECVD) ▪ High-Density Plasma CVD (HDPCVD)	Low temperature, fast deposition, good step coverage, good gap fill.	Requires RF system, higher cost, much higher stress with a tensile component, and chemical (e.g., H_2) and particle contamination.	High aspect ratio gap fills, low-temperature oxides over metals, ILD-1, ILD, a copper seed layer for dual damascene, passivation (nitride).

In the next two subsections, LPCVD and PECVD processes are described in detail. Since these two processes are required to form a pocket implanted MOSFET structure. After that, the formation process of the pocket implant MOSFET will be described step by step.

C.1 LPCVD process

Low-Pressure Chemical Vapor Deposition (LPCVD) systems are frequently used deposition techniques due to their lower cost, higher production throughput, and superior film properties. LPCVD operates at a medium vacuum pressure of about 0.1 to 5 Torr, and high temperature in between 300 to 900^0C (C. Y. Lu and J. M. Sung, 1989). Conventional oxidation type furnaces (either horizontal or vertical) and multi-chamber cluster tools can be used for LPCVD processing.

LPCVD reactors characteristically function in the reaction-rate limited regime. In this reduced-pressure range, the diffusivity of the reactance gas molecules rises. Therefore, the mass-transfer of the gas to the wafer cannot set a barrier to the upper limit of the reaction rate. However, due to this mass-transfer rate, the gas-flow situations inside the reactor are no longer a prime factor, and thus it permits the reactor designer to optimize it for the high wafer capacity, for example, wafers now can be closely placed. After that, the films are homogeneously doped on a huge number of wafer surfaces as long as the temperature is strongly controlled. The reaction rate bounds the deposition rate, but not the reactant supply. There are many collisions during LPCVD so that material strikes the wafer in an undirected manner. This action is beneficial for conformal film coverage on high aspect ratio steps and trenches.

There are numerous applications for LPCVD oxides (doped and undoped) in ULSI multilevel metallization. LPCVD oxides are used for Inter-Layer Dielectric (ILD), Shallow Trench Isolation (STI) oxide fill, and sidewall spacers.

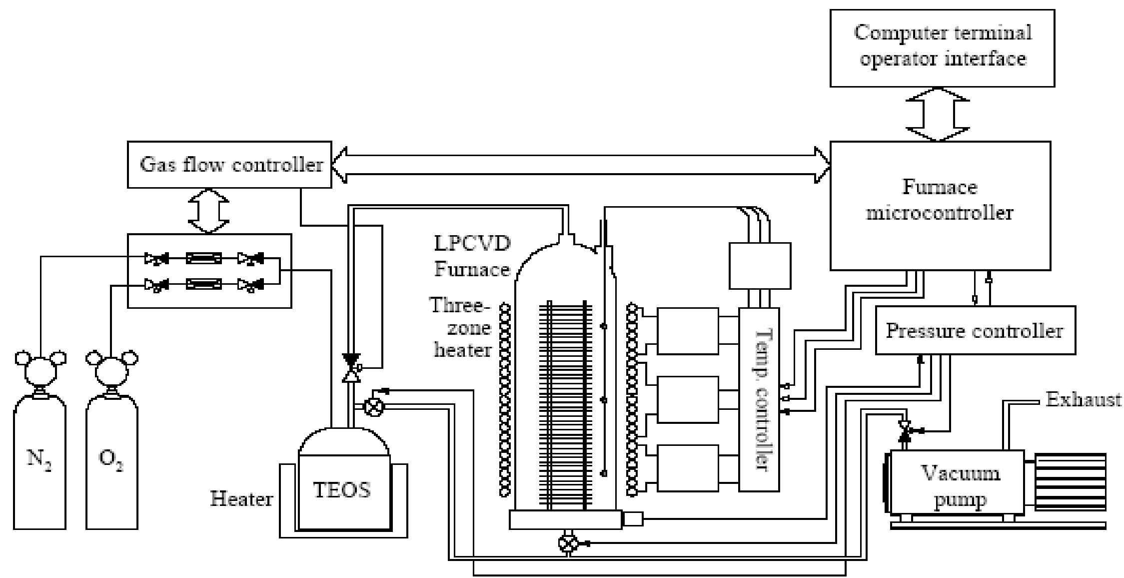


Figure 5: Oxide depositions with TEOS LPCVD

A common LPCVD method for depositing SiO_2 is the pyrolysis/decomposition of TEOS with or without oxygen at low pressure and a temperature between 650^0 to 750^0C. This method is sometimes referred to as LPTEOS, for low-pressure TEOS. LPTEOS yields very good oxide conformity due to the rapid surface diffusion of gas molecules. A liquid TEOS source is used by bubbling a carrier gas through it (e.g. N_2, O_2, or He). The liquid source is heated by its independent temperature source. The concentration of the liquid source vapor entering the reactor is controlled by the carrier gas flow rate and liquid source temperature. A schematic of a typical TEOS deposition system is shown in Fig. 5. The film growth rate for LPCVD oxides is significantly slower (10-15 nm/min) than for APCVD films (Y. Okumura *et al*, 1990).

C.2 PECVD process

The development of Plasma Enhanced Chemical Vapor Deposition (PECVD) expends plasma energy to create and sustain the CVD reaction. It is a natural follow-on to LPCVD since the system pressure for both types of CVD processes is equivalent. The important difference is that the deposition temperature is very much low in the PECVD method. For instance, Si_3N_4 can be deposited using the LPCVD process at 800^0 to 900^0C, but cannot be deposited over Al metallization because Al melts at 666^0C. On the other hand, Si_3N_4 can be deposited with the PECVD method at a temperature of 350^0C very easily for the same application (J. R. Brews *et al*, 1980).

PECVD is performed in a vacuum chamber between parallel conducting plates positioned several inches apart, typically with a variable gap for process optimization. A modern reactor is a multi-chamber cluster tool. The wafer is placed on the grounded lower plate and radio frequency (RF) heat is supplied to the upper electrode. Plasma develops at the time the source gas is supplied through the gas manifold and the center of the electrodes. Exhaust gases are then pumped out from the periphery of the lower electrode. Sometimes the reactant gases are introduced at the periphery and pumped out at the center of the lower electrode. The schematic of an overall PECVD system is presented in Fig. 6.

Oxide films with PECVD are usually formed by reacting silane (SiH_4) with either oxygen (O_2), nitrous oxide (N_2O), or carbon dioxide (CO_2) in plasma. The processing temperature is about 350^0C. The oxide can be doped with boron or phosphorous to form BSG or PSG, respectively, or with both to deposit BPSG. PECVD PSG tends to be more crack-resistant, conformal, and free of pinholes than APCVD PSG.

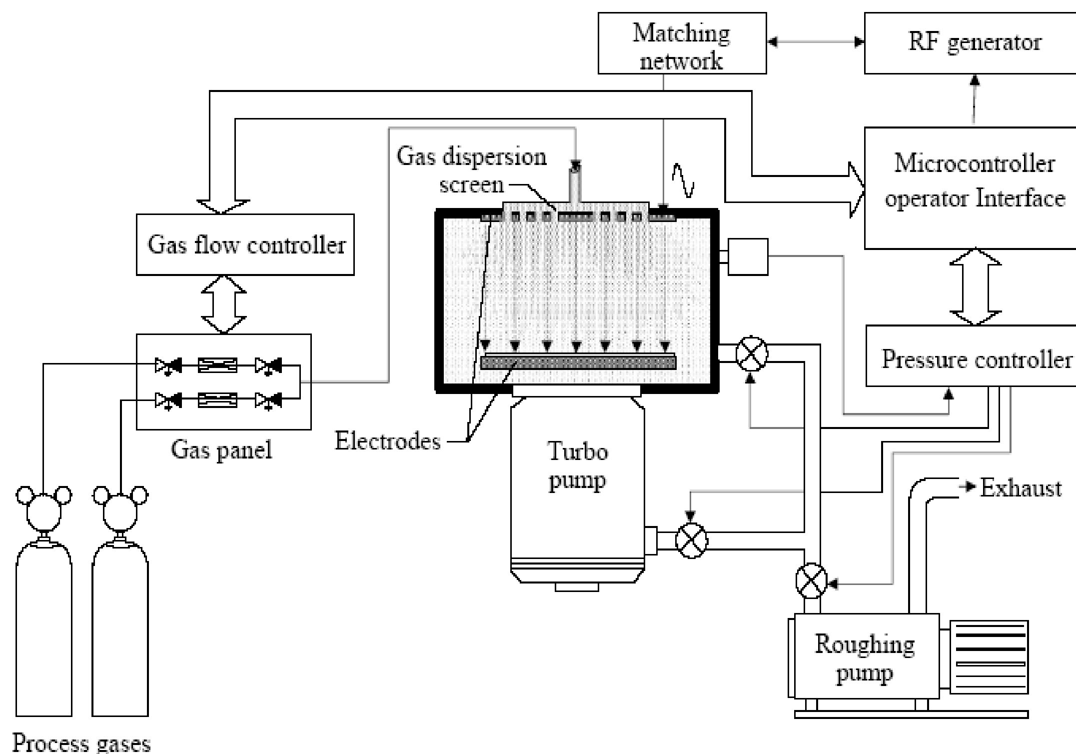


Figure 6: General schematic of PECVD

D. Reactive Ion Etching Techniques

Reactive Ion Etching (RIE) is a kind of etching technique utilized in the semiconductor fabrication industry at the micron level (J. R. Brews *et al*, 1980). In this technique, chemically reactive plasma is employed to eliminate a particular material deposited on the wafers. This plasma is produced at low pressure typically less than 0.1 Torr in vacuum by applying an electromagnetic field, which sends the high-energy ions from the plasma. Then these ions attack the wafer surface and react with its material to be removed.

A typical parallel plate RIE system is shown in Fig. 7. It comprises a cylindrical vacuum chamber, with a wafer platter placed in the lower part of the chamber. It is mainly kept grounded and is electrically isolated from the remaining portion of the chamber. The gas passes into the chamber via a small inlet at the top of it and leaves to the vacuum pump structure from the bottom of it. The types and amount of gases to be used in the chamber differ as per the etching method; for example, sulfur hexafluoride gas (SF_6) is generally used for etching Si. Gas pressure is normally retained within a few millitorrs to a few hundred millitorrs through the regulation of the gas flow rates and/or the alteration of an outlet.

Various other types of RIE systems are available, including Inductively Coupled Plasma (ICP) RIE. In the ICP-RIE system, the plasma is produced in an RF powered magnetic field to achieve a very high plasma density to have an isotropic etch profile.

On the other hand, a parallel plate and an inductively coupled plasma RIE technique are also available. Here, the inductively coupled plasma (ICP) is utilized to provide the high-density source of ions to get an enhanced etching rate. However, a separate RF bias voltage is applied to the substrate i.e., the Si wafer to get directional electric fields in the close vicinity of the substrate to attain more anisotropic etch profiles (T. Hori, 1994).

After that, the plasma is prepared in the system with the application of a strong Radio Frequency (RF) field at the wafer platter. The field frequency used here is 13.56 MHz with a few hundred watts of electric power. This high-

frequency oscillating nature of the electric field ionizes the gas molecules by disrobing them of electrons and thus producing the plasmas.

In each half-cycle of the oscillating electric field, the electrons are accelerated in the upward and downward directions inside the chamber. In this process, it sometimes strikes the upper wall of the chamber and sometimes the wafer platter. In the meantime, the relatively heavier ions move comparatively small distances responding to the RF electric voltage. As soon as the electrons are absorbed into the chamber walls, they are passed to the ground terminal and cannot vary the electronic configuration of the system. However, the absorbance of electrons into the wafer platter causes it to accumulate charges because of its DC isolation. The accumulated charges develop a huge negative voltage on the platter, usually of the order of a few hundred volts. Of course, the plasma itself grows a slightly positive charge because of the greater concentration level of the positive ions as compared to the free electrons.

Due to the enormous voltage difference, positive ions drift down the wafer platter and then they collide with the samples/materials are to be etched. These ions have chemical reactions with the materials on their sample surfaces. However, this can knock-off/sputter some of the material by transporting a portion of their kinetic energy. Most of the distribution of reactive ions is mainly vertical, and hence the RIE technique yields very anisotropic etching profiles. This is in contrast with the classical isotropic profiles that we can have from wet chemical etching.

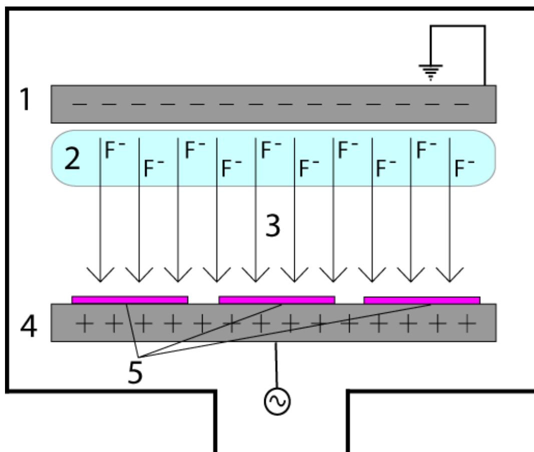


Figure 7: Parallel-plate RIE reactor

The conditions of the chemical etching process of an RIE system depend mainly on the process parameters, for example, applied pressure, gas flow rate, and RF power level.

E. Annealing Process

Ion implantation damages the Si lattice by knocking atoms out of the lattice structure. With a high dose, the implanted layer becomes amorphous. Furthermore, the implanted ions rarely enter the lattice structure sites of the Si, instead of stopping in interstitial sites outside the lattice. These interstitial dopants are electrically inactive until activated by a high-temperature annealing step. Annealing heats the implanted Si substrate to repair crystalline damage and electrically active dopants by moving the atoms into crystal lattice sites as shown in Fig. 8.

Crystal damage repair is done at about 500^0 C and dopant activation occurs at about 950^0C Electrical activation of dopants occurs as a function of time and temperature, with longer times and higher temperatures increasing the dopant activation (J. R. Brews *et al*., 1980).

There are two basic methods for heating the implanted wafer for anneals:

- Furnace anneal
- Rapid Thermal Anneal (RTA)

Furnace anneal: It is the traditional method of annealing by heating the wafer in a hot-wall furnace in the range of 800 to 1000^0C for about 30 minutes. At this temperature, the Si atoms move back into the lattice sites and the dopant atoms come into the substitutional sites inside the lattice. However, annealing cycles at this time and temperature can cause extensive dopant diffusion and is undesirable for advanced IC wafer fabrication (J. R. Brews *et al*., 1980).

Rapid thermal anneal: Rapid thermal anneal anneals the wafer by using an extremely fast ramp and short dwell time at the target temperature (typically 1000^0C). Annealing of implanted wafers is usually done in a single-wafer rapid thermal processor (RTP) with argon (Ar) or nitrogen (N_2) flowing into the chamber. A fast ramp rate and short dwell time is optimized to anneal the wafer to restore lattice damage and electrically activate the dopant while minimizing dopant diffusion in

the Si. RTA also minimizes a phenomenon known as transient enhanced diffusion. RTA is the optimal annealing method to achieve acceptable junction depth control in shallow implants (J. R. Brews *et al.*, 1980).

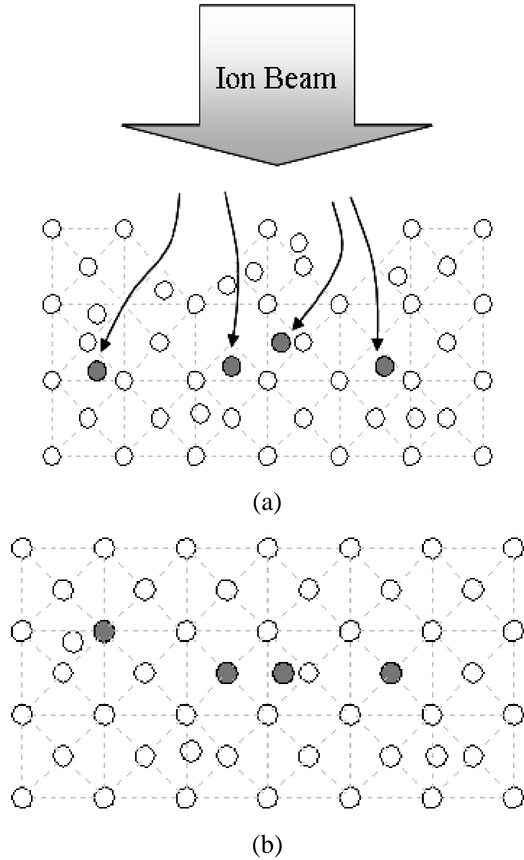


Figure 8: Annealing of Si Crystal: (a) Damaged Si lattice during implant; (b) Repaired Si lattice structure and activated dopant-Si bonds after annealing

Investigations have been done into spike anneals for RTA. The ramp-up rate is very fast at up to 150^0C/s. This speed permits a soak time reduction to about 1 s. Uniform ramp rates during a spike anneal are critical because much of the thermal exposure occurs during the ramp.

There are different types of heating, with a common method being tungsten halogen lamps positioned on both sides of the wafer. Multiple optical pyrometers are often used to measure temperature across the wafer to ensure uniformity.

III. Pocket Implanted MOSFET Structure

The development of nano-scaled MOSFETs has compelled the semiconductor device designers to engineer the source/drain regions to form halo or pocket implanted regions at the surface, i.e. near the channel area. The structure of the pocket implanted MOSFET device is very much similar to that of a bulk MOSFET. It differs only in the pockets created adjoining to the greatly doped source and drain borders of the channel located at the surface of the device. These regions are formed in such a way that they have equal conductivity and type as the substrate or well region of the device. However, the pockets have a higher level of doping concentration than those in the substrate or well region. These variations of doping density in the pocket implanted MOSFET device structure diminish the penetration depth of the depletion region towards the MOSFET substrate. This lower penetration depth of the depletion regions yields less punch through current through the reverse-biased junctions. Of course, the augmented dopant density of the pocket region badly impacts the MOSFET performances due to the elevated junction capacitance in the short channel MOSFETs. Hence the device designers need to trade-off between the diminished punch through current and enlarged junction capacitance. Like a conventional bulk MOSFET device, the pocket or halo implanted MOSFET device is also two types- p-type and n-type based on its channel carrier's type. There are various methods or processes of fabricating the pocket or halo implanted n- or p-type MOSFET structures. In the following two sub-sections, the fabrication processes of these two types, one for p-type halo implanted and another for n-type pocket implanted MOSFET device structures are described from the published papers of J.-G. Su *et al.*, 1997 and E. Quek, 2005 respectively.

A. Formation of the Halo PMOS

The process flow used in forming the halo p-type MOSFET device is abridged in Table 5. The icon '*' in the halo-implant area indicates the parameter that is to be attuned.

J.-G. Su *et al.*, 1997 in their work has designed the halo-implanted MOSFET structure using the numerical device simulator- MEDICI. Then this device is simulated to get device structure and its vertical cross-section with doping concentration contours is revealed in Fig. 9 and its various split conditions are presented in Table 6.

Table 5: The Process Flow

Process Step	Process Conditions
p-type formation	<100>, B, 1.3×10^{15} cm^{-3}
n-well formation	Material/dose/energy P/1.3×10^{13} cm^{-2}/460 keV
Channel implant	Material/dose/energy P/2.0×10^{12} cm^{-2}/40 keV
Gate oxide	Thickness: 5.5 nm
Poly deposition	Thickness: 0.1 µm/length 0.18 µm
Halo implant	Material/dose/energy/tilt As/* cm^{-2}/130 keV/* deg
LDD implant	Material/dose/energy BF_2/1.0×10^{13} cm^{-2}/25 keV
Spacer formation	Length 0.08 µm
P^+ S/D implant	Material/dose/energy BF_2/2.0×10^{15} cm^{-2}/30 keV

The effect of variations of the tilt angle, including 0^0, 15^0, $30^{0,}$ and 40^0 have been studied with several halo implant ion doses to examine their performance boundary. All halo implants are formed with the implantation energy of 130 keV. The gate length of the device is 0.18 µm, gate oxide thickness of it is 5.5 nm, Lightly Doped Drain (LDD) region's ion dose level is 10^{13} ions/cm^{-2} at the energy of 25 keV, and nitride spacer thickness is 0.08 µm. The process simulator TSUPREM4 (E. Quek, 2005) and device simulator MEDICI (TMA, 1999) were used in this analysis.

From these experimental and simulation results, it is revealed that the larger tilt angle should be used for the halo implantation process to obtain less parasitic capacitance and thus to achieve the superior performances of the MOS devices having the channel length in the nano-scaled regime.

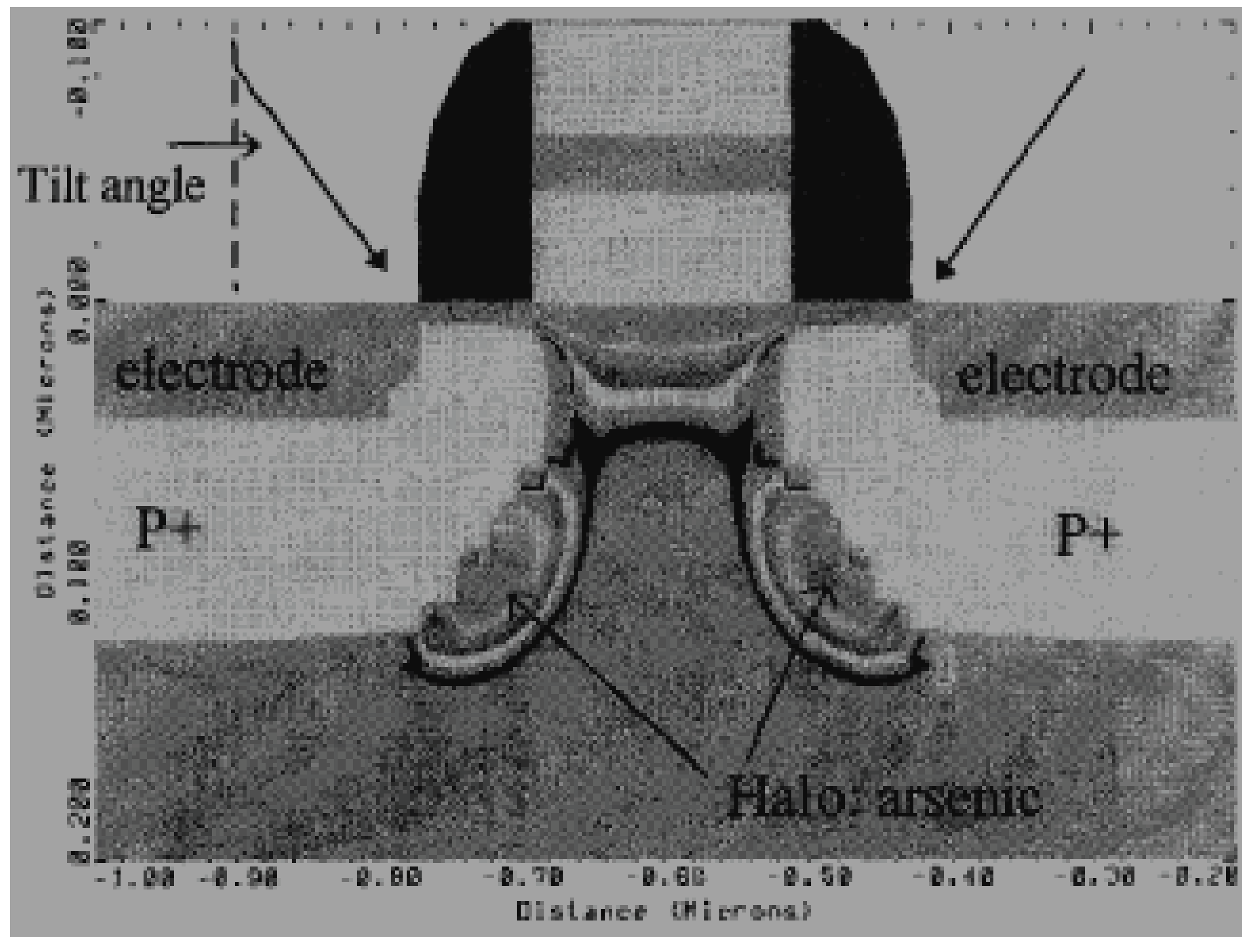


Figure 9: The Halo PMOS cross-section (adapted from J.-G. Su *et al*., 1997)

Table 6: The split conditions

Split Number	Halo Implantation Condition	
	Dose #/cm^2	Tilt Angle (Degree)
A	3×10^{12}	0^0
B	7×10^{12}	
C	9×10^{12}	
D	1×10^{12}	15^0
E	3×10^{12}	
F	5×10^{12}	
G	1×10^{12}	30^0
H	2×10^{12}	
I	3×10^{12}	
J	5.2×10^{12}	
K	8.5×10^{11}	40^0
L	1×10^{12}	
M	2×10^{12}	
N	3×10^{12}	

B. Formation of the Pocket Implanted n-MOSFET

The process for forming a pocket implanted MOS device is to place the pockets contiguous to the sides of a source/drain at the surface area of a semiconductor substrate where an inversion channel is created. But the pocket regions are not directly under the gate material or the composite insulator spacers, which are at both sides of the gate material. The formations of different regions of the device are shown inside the constructed structure by numbers in Fig. 10 and are expressed in parenthesis while referring to the texts.

At first, a semiconductor substrate (1) is taken. It is a single p-type Si crystal oriented at the <100> direction. After that, a SiO_2 layer is formed as the gate insulator (2). This layer may be formed by using a thermal growth technique through the oxidation process having an oxide thickness of 1 to 2 nm approximately. However, silicon nitride (Si_3N_4) or a nitride oxide gate insulator may also be formed through the annealing process of a base silicon di-oxide (SiO_2) deposit in a nitric oxide (NO) or nitrogen dioxide (NO_2) environment. Besides, hafnium oxide (HfO_2) or any such type of high-*k* dielectric material may also be utilized as the gate insulator layer.

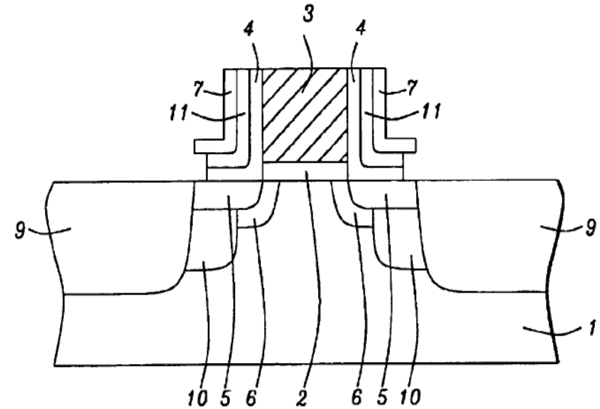


Figure 10: Pocket implanted n-MOSFET structure with composite insulator spacers (E. Quek, 2005). Various regions' numbers are shown in the text

After the formation of the gate oxide layer, a conductive layer needs to be created on the gate insulation layer to build the contacts, viz., a doped polysilicon coating, or a metal silicide coating having a depth of around 100-250 nm. If a doped polysilicon layer is to be formed then we may use the Low-Pressure Chemical Vapor Deposition (LPCVD) technique or Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. In both of these techniques, the polysilicon layer doping process is performed in situ via the accumulation of arsine (AsH_3) or phosphine (PH_3) in the silane (SiH_4) or di-silane (Si_2H_6) ambient.

The gate structure region (3) is defined in the conductive layer. In this stage, photolithographic and anisotropic reactive ion etching techniques are used with chlorine (Cl_2) or Sulphur hexafluoride (SF_6) as an etchant material. The photoresist that defines the gate structure is removed using oxygen (O_2) ashing and wet clean techniques with the buffered hydrofluoric (HF) acid. After that, a thermal oxidation step is employed to develop the silicon dioxide (SiO_2) layer at the region (4) on the uncovered surface area of the gate structure having a thickness of between 1 to 3 nm.

In the next step, an n-type Lightly Doped Drain (LDD) zone (5) is formed using the ion implantation procedure with an implant energy of 1-10 keV and implant dose of around 3×10^{13}-3×10^{15} atoms/cm^2 of arsenic (As) ions. However, we may wish to use phosphorous (P) ions as an alternative source. But these ion-implanted regions must be created in the semiconductor substrate

areas close to the source and drain sections that are not shielded by the gate structure.

To inhibit the impingement of the Solid Phase Epitaxial (SPE) depletion layers, a shallow pocket is formed at the drain side or both at the drain and source sides (6) right after the LDD region (5). The key features of the pocket regions are that they must have the same conductivity and type as that of the semiconductor substrate with a higher doping level than that of the substrate. This layer is designed in such a way that it wraps the entire n-type LDD region (5). Since the substrate is p-type, therefore the pocket regions (6) are also p-type. The pocket regions (6) are also created using an ion implantation process using boron (B) ions from the boron fluoride (BF_2) ion source at an energy between 7-15 keV with an ion dose of about 2×10^{13}-7×10^{13} atoms/cm^2. The entire process is executed in situ, either before or after the formation of the n-type LDD region.

After that, a composite insulator spacer is made on both edges of the gate structure (3). At first, a SiO_2 layer (11) is placed at a thickness of 8-15 nm employing either LPCVD or PECVD technique with tetra-ethyl-ortho-silicate (TEOS) as a source. At the second step, the silicon nitride (Si_3N_4) layer (7) is placed at a thickness of 15-30 nm employing again the LPCVD or PECVD technique. At the third step, silicon dioxide (SiO_2) layer (8) is put having a thickness of 40-70 nm utilizing the LPCVD or PECVD technique again with tetra-ethyl-ortho-silicate (TEOS) as a source and using CHF_3 as an etchant for SiO_2 and Cl_2 s an etchant for Si_3N_4 engaging anisotropic RIE procedure.

In the next stage, strongly doped n-type source and drain regions (9) is designed in semiconductor surface zones that are not enclosed by the gate structures or by the composite insulator spacers. These regions are also implemented by employing the ion implantation technique with As or P as the ion sources at an energy level between 35-75 keV and an ion dose level between 2×10^{15}-7×10^{15} atoms/cm^2. This stage is followed by an additional ion implantation technique engaging phosphorous (P) ions at an energy level in between 25 to 45 keV with ion dose in between 1×10^{13}-4×10^{13} atoms/cm^2. This step is followed in an intention to reduce the junction capacitance. Another important parameter during the ion implantation process is its tilt angle. It is kept in between 0^0-7^0 during this ion implantation process to have the graded dopant profiles of n^+/p well.

After the implementation of the source and drain regions, a deeper p-type pocket region (10) is implanted to diminish the punch-through current aroused from the depletion regions. The doping is p-type in this region 10 and its concentration is also higher than that in the p-type semiconductor substrate. This process is performed by using the ion implantation technique. Boron (B) is implanted as a p-type dopant from the boron di-fluoride (BF_2) as the ion source at an energy level of between 21-31 keV with an ion dose of roughly in between 3×10^{13}-8×10^{13} atoms/cm^2 and with a tilt angle of around 10^0-30^0. The implantation energy is selected in a way that the p-type dopants penetrate along the horizontal path of the L-shaped silicon nitride (Si_3N_4) spacer region (7) and the areas underneath the silicon dioxide (SiO_2) layers (11) and (4). In addition to that, the implant dose is high enough to create a deep p-type pocket implanted region (10) in the exposed areas of the lightly doped shallow p-type pocket region (6). However, the implanted ion dose is not enough to compensate for the heavily doped n-type source/drain regions (9) fully. This yields in p-type pocket implanted regions located neighboring only in the sides of the strongly doped n-type source/drain regions (9). Some areas of the n-type LDD region (5), shrouded by the p-type pocket implant section (6) having low depth and situated beneath the L-shaped Si_3N_4 spacer segment perpendicular to it, remain uncompensated and hence directly impact the channel length/width of the MOS structure.

In the final stage, an anneal process, executed via rapid thermal annealing (RTA), is used at a temperature between 1050 to 1090^0 C for a period of around 0-15 s in a passive ambient to actuate all the entrenched ions in the device.

C. Characterization of Pocket Doping Profile

As MOSFETs were started to scale down below the 100 nm of the channel length, the two-dimensional distribution of doping concentration became dominating and was disturbing its various characteristic parameters. As such, to enhance the level of performance of the various parameters of

the MOSFETs, various techniques were employed since then. One such effort is to have the Reverse Short Channel Effect (RSCE) (M. Nishida and H. Onodera, 1981) in the channel. This is found due to the enhanced diffusion of dopant atoms adjacent to the source/drain junction areas (M. Nishida and H. Onodera, 1981; TMA1, 1994; P. C. Zalm, 1993). After that, another development of devices was observed. This is the lateral engineering of the impurity atoms' profile along the channel from the source/drain regions toward its center at the surface of the device substrate. In this method, the lateral doping profiles along the channel are the implantation of pockets or halos (B. Yu *et al.*, 1997). However, this method requires a solid apprehension of the dopant atoms diffusion process in 2-dimension during the device fabrication process of such advanced MOSFET devices. However, we also need to know the application areas, such as process calibration, monitoring, and troubleshooting. Besides, knowledge of device design and optimization is also indispensable. To know the exact doping profiles, we need to characterize the MOSFET devices.

Device characterization is defined as the quality of the device in terms of its parameters. It is an activity right after the device design, development, and implementation. In the same way, the design verification is another activity right after the device design processing and validation of the models right before the design phase (M. H. Bhuyan *et al*, 2011).

To determine one-dimensional (1-D) doping profiles, various procedures were evolved and were implemented. Of them, different capacitance-voltage (*C-V*) methods (S. M. Sze, 2001) and Secondary Ion Mass Spectroscopy (SIMS) techniques (P. C. Zalm, 1993) were the most popular. However, the SIMS technique is destructive and time-consuming. Therefore, a few indirect techniques were also developed. One such technique is inverse modeling. In this method, a doping profile is obtained to match the results of its numerical simulations of the electrical behavior with its experimental data (G. J. L. Ouwerling, 1991; N. Khalil *et al*, 1995; Z. K. Lee *et al*, 1999). Extraction of the 2-D doping profiles from the *C-V* data was also found in the literature (G. J. L. Ouwerling, 1991; N. Khalil *et al*, 1995). As the device dimensions are going down in the nano-scale regime, the device capacitances of are being also diminishing. As such, the distinctive test and measurements are getting obligatory. The noise of the device became a vital parameter for such cases.

The Scanning Capacitance Microscopy (SCM) is a direct technique that can determine the 2-D doping profiles in conjunction with the Atomic Force Microscopy (AFM) technique. This is one of the most dominant techniques to characterize semiconductor MOSFET devices. This method has received popularity due to its non-destructive nature and having extraordinary spatial resolution down to 1 nm (M. H. Bhuyan *et al*, 2011). A 0.15 μm channel MOSFET was detected using this direct SCM method for the first time as per record found in the literature (R. N. Kleiman *et al*, 1997).

However, currently, VLSI/ULSI technology emphasizes an accurate understanding of the spatial extent in three dimensions (3-D) of active dopant atoms that have been assimilated into the discrete device components. The active part of the device is engineered by introducing dopant atoms, viz., B, As, Sb, or P with a concentration from 10^{15} to 10^{20} atoms/cm^{-3}. In the 2-D junctions of a device having channel length in the sub-100 nm regime, it is essential to enumerate the deviation of these doping profiles in terms of its resolution in the range of 100 nm or less. Having extremely precise doping profile characterization is a significant undertaking in both the device design and manufacturing stages.

Therefore, the dopant profiles measurement and characterization method should be very simple, direct, upfront, reliable, accurate, precise, reproducible, and non-destructive in 2-D or even in 3-D. Lateral doping profiles were confirmed from the capacitance measurement and simulation (W. Rosner *et al*, 1990), or junction-staining (S. T. Ahn and W. A. Tiller, 1988). A 'tomographic' technique utilizing the SlMS measurement was investigated (S. H. Goodwin-Johnson *et al*, 1989). The Scanning Capacitance Microscopy (SCM) and the Atomic Force Microscopy (AFM) (J. R. Matey and J. Blanc, 1985; C. C. Williams *et al*, 1989) techniques can jointly measure the 2-D and 3-D lateral doping profiles' images (C.C. Williams *et al*, Oct. 1989; D. W. Abraham *et al*, 1997).

However, according to the literature, a few researchers used the Scanning Tunnelling Microscopy (STM) method on p-n junctions (S. Hosaka *et al*, 1988; S. Kordic *et al*, 1989).

The Scanning Capacitance Microscopy (SCM) is currently being employed to get the image of the dopant gradients in Si and other semiconductor devices. This is a non-destructive and contactless method with which the local variations of quality in the dielectric thin films and the properties of the semiconductor substrates can be investigated properly (M. H. Bhuyan *et al*, 2011). However, any kind of measurement that can be performed with the fabricated metal like electrodes can also be determined with the SCM technique.

IV. Conclusions

Due to device dimension shrinking, many advanced devices are being evolved. As such, the semiconductor device engineers are in search of various device design, simulation, and implementation techniques. Therefore, the researchers are investigating these issues. Since device fabrication techniques are very expensive, therefore, before adopting any method for a novel device, it is imperative to investigate whether the existing available technologies are useful for this device manufacturing or not.

The pocket or halo implanted MOSFET is the novel semiconductor devices in the nano-scaled regime to combat the Short Channel Effect (SCE) by embedding the Reverse Short Channel Effect (RSCE) through lateral channel doping profile engineering. Therefore, it is necessary to investigate its suitable fabrication processing methods from the existing techniques. In this article, fabrication technologies at several stages of pocket implanted n-MOSFET structure and halo p-MOS devices are explained in detail.

However, to know the precise doping profile of the fabricated devices, the characterization of it is another important area to be explored for the nano-scaled devices. Therefore, a lateral doping profile technique named Scanning Capacitance Microscopy (SCM) is suggested for such devices.

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