A Comparative Study on Various Recent Single-Phase Single-Switch Non-Isolated AC-to-DC SEPIC Configurations

Istiak Ahmed and Muhibul Haque Bhuyan

Abstract**—**In this comparative analysis-based research paper, five recent power electronic circuits of single-phase, non-isolated AC-to-DC SEPIC configurations are considered, such as, switched capacitor, modified, high-efficiency, input switched, and improved performance based SEPIC circuits. The open-loop performance analyses were made among these five recent converter circuits. Before that, a good number of articles on power electronic converter circuits are studied and key performance parameters, for example, voltage gain, efficiency, power factor of the supply current signal, Total Harmonic Distortion, and the number of parts were identified. Then these are analyzed based on the variation of load resistance and duty cycles. The performance evaluation points out that the high-efficiency SEPIC circuit provides an impressive efficiency of over 99% within a wide range of load resistances or duty cycles. In terms of power factor, the modified SEPIC circuit demonstrates better results of over 0.98. The switched capacitor SEPIC circuit can provide the lowest THD among the five topologies.

Keywords**—**SEPIC topology, duty cycle, load, switching frequency, total harmonic distortion, voltage gain.

I. Introduction

As the industrial growths are going on in full swing, dependable, efficient, compact-sized, and superior voltage conversion circuits are gaining importance, As such, some of the power electronic converter circuits, especially the AC-to-AC, DC-to-DC, AC-to-DC, or DC-to-AC types of conversion circuits have become very significant. Each circuit has several topologies that can be found in the literature. The changes in the design of such topologies can bring significant changes in their performance parameters and make them suitable for particular applications [1-2].

Usually, a buck converter lowers the DC signal level [3], a boost converter raises the DC signal level [4], and a buck-boost converter can do both [5]. All such converters are a kind of DC-to-DC converter. When such converter lowers or raises the voltage level from its supply-side to its load side then the current level is automatically raised or lowered down respectively. The converter has a minimum of 2 electronic devices, like a diode and a transistor though the recent converters contain only the transistors for the synchronous operation along with the energy-storage element, like capacitor, inductor, or both. Filter circuits are used to curtail the ripples either at the input or at the output side. The main element of the filter circuit is a capacitor, an inductor, or both when it is passive type. When such filters are used in the power electronic circuit, this not only suppresses the ripples but also improves the power factor, wave shapes, and voltage gain [6-8].

However, there are some problems associated with the use of capacitors in the AC-to-DC rectifier circuits, such as high current harmonics, which is not within the acceptable range of international regulations. The purpose of using the capacitor is to filter out ripples of the rectification circuitry but this capacitor draws the peaked current merely for a very small period in a particular half-cycle of the signal to charge the capacitor. As such, the current taken by the AC-to-DC rectifier circuits also become non-sinusoidal and thereby creates harmonics. Therefore, a DC-to-DC conversion circuit is utilized at the load side of the rectifier to keep track of the supply voltage by the input current via a control scheme, which is an imitation of the complete resistive mode activities of the rectification circuit [9]. A conversion circuitry with this organization is called the Power Factor Pre-Regulator (PFP) configuration.

In the literature, there are various kinds of PFP circuits apart from the Buck, Boost, and Buck-Boost circuits, for example, the Cuk [10], and Single-Ended Primary-Inductor Converter (SEPIC) [11-13] configured circuits. The most commonly employed PFP is a boost converter due to its modest configuration [14], but it has several drawbacks, such as non-availability of the high-

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frequency isolation, high level of starting current, no overload protection, etc. [15].

There are two control modes of such converters, such as 1) Continuous Conduction Mode (CCM) and 2) Discontinuous Conduction Mode (DCM) [5, 16-17].

There are numerous benefits of employing the SEPIC circuit topology in the power electronic circuit, for example, if it is operated in DCM with properly selected inductance values then a pure sinusoidal input current is possible to obtain [10-13]. Besides, its output voltage is the non-inverting type [18]. By harnessing such benefits, in many power electronic applications, the SEPIC circuit has been employed. In one such literature, it was found that a 28V, 1 kW converter was designed with a variable input voltage of 230 V ± 15% and variable supply frequency from 360 Hz to 800 Hz to apply it in aircraft. To test the system performance, MATLAB/Simulink model was developed for both transient and steady-state conditions [19].

SEPIC circuits were utilized in a 1 kW solar panel and then simulated using MATLAB/Simulink for stand-alone photovoltaic (PV) systems [20-21]. Besides, a Fuzzy Logic Controller (FLC) based SEPIC circuit was designed, implemented, and tested for Maximum Power Point Tracking (MPPT) of a PV-based scheme to obtain the faster response time, high precision level, the constant voltage at variable load conditions, smaller steady-state error and overshoot, high efficiency, optimal use of PV array, unity load power factor, etc. The scheme was materialized using a Digital Signal Processor (DSP) of Texas Instruments (TI), TMS320F28335 [22].

In another paper, the diode was substituted by a MOS device to obtain the reduced voltage drop matched to the diode to yield greater efficiency of the circuit [23].

The Pulse Width Modulation (PWM) technique-based SEPIC-fed Light Emitting Diode driver circuit was designed and tested in a paper to have high brightness, better power quality, lower power factor, and better Total Harmonic Distortion (THD) in an LED operated projection application. The scheme is used as a Power Factor Corrector (PFC) that works in the Discontinuous Current Mode (DCM) [24].

In another paper, it was demonstrated that with the use of SEPIC circuit in modeling and simulating the Wind Energy Conversion System (WECS) in MATLAB under fluctuating environments, the lower harmonic contents of the generator was reduced while the output power level improved by 4-8% and overall efficiency was raised to over 94% with 3-level Neutral Point Clamped (NPC) inverter linked to the grid concerning the conventional boost converter circuit [25].

This review paper aims to analyze various types of Single-Ended Primary-Inductor Converter (SEPIC) topologies based on the PSIM simulator.

II. Topologies and Operations of the AC-to-DC SEPIC Circuit

AC-to-DC converters convert the input AC to output DC. These converters are classified based on their respective voltage gain characteristics. Generally, buck converters are used when we need to lower the input voltage and Boost converters are used when we need to raise the input voltage level at the output side. There are other converters like buck-boost, Cuk, SEPIC, and Zeta which can perform both step-up and step-down operations depending on the duty ratio. New topologies of buck-boost [26-27], Cuk [28], and Zeta [29-30] converters have been developed to provide higher efficiency and better power factor than the conventional converters. Over the past decades, many alterations were made to improve the performances of the conventional AC-to-DC SEPIC topologies. In the next five sub-sections, a comparative review of the five diverse structures of recent single-phase single-switch non-isolated AC-to-DC SEPIC circuits has been provided. The open-loop analysis of the single-input, single switch SEPIC topologies is done using PSIM version 9.1.1.

A. *Switched Capacitor AC-to-DC SEPIC Circuit*

The drawing of the switched-capacitor AC-to-DC SEPIC circuit is presented in Fig. 1. Three inductors (L_1-L_2 and L_{in}), five capacitors (C_1-C_4 and C_{in}), eight diodes (D_1-D_8), and a unidirectional switch (M_1) are the main components of this circuit. At first, there is a basic 1-ϕ rectifier circuit using four diodes (D_1-D_4). Then a modified switched capacitor DC-to-DC converter is cascaded with it to be operated at high frequency. Inductors, L_1, and L_2 work as SEPIC inductors. Inductor, L_{in} and capacitor, C_{in} constitute the passive filter circuit at the input. Capacitor, C_1 forms the output filter and resistor, R_1 resistor acts as the load [31].

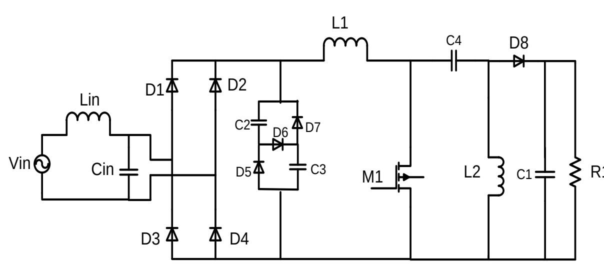

Fig. 1. Switched capacitor AC-to-DC SEPIC circuit [31]

Circuit parameters and their values used in this circuit are as follows:

The peak source voltage (V_{in}) applied to the circuit is 300 V with a frequency of 50 Hz. The MOS device, M_1 was used for the switching purpose. The values of inductors L_1 and L_2 are 400 µH each and that L_{in} is 40 mH. Capacitors C_2 to C_4 have values of 1 µF each and C_{in} and C_1 have values of 50 µF each. The load resistor R_1 is 100 Ω [31].

B. Modified AC-to-DC SEPIC Circuit

The drawing of the modified AC-to-DC SEPIC circuit is depicted in Fig. 2. The circuit includes five diodes (D_1 to D_5), four inductors (L_{1+}, L_{1-}, L_{if}, and L_2), four capacitors (C_{if+}, C_{if-}, C_1, and C_2), a switch (S), and a resistive load (R_L). An inductor (L_{if}) and a capacitor (C_{if}) form the input filter. An inductor L_{1-} is employed in the series path to facilitate current flow when it goes into the negative half cycle of the source voltage [32].

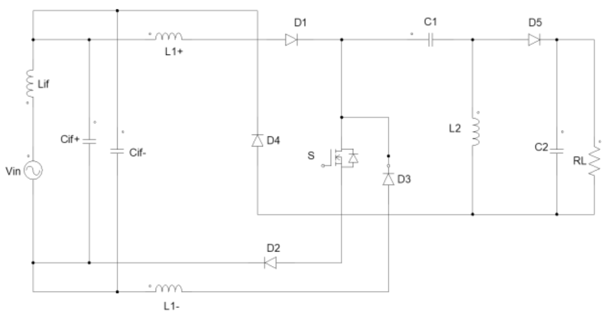

Fig. 2. Modified AC-to-DC SEPIC circuit [32]

Circuit parameters and their values used in this circuit are as follows:

The peak source voltage (V_{in}) applied to the circuit is 300 V with a frequency of 50 Hz. An IGBT has been employed as a switching device. The inductance values of different inductors of this circuit are $L_{1+} = L_{1-} = 2$ mH, $L_2 = 2$ mH and $L_{if} = 5$ mH. The capacitance values of different capacitors are $C_{if+} = C_{if-} = C_1 = 1$ µF, and $C_2 = 20$ µF. The load resistor R_L is 100 Ω [32].

C. High-Efficiency AC-to-DC SEPIC Circuit

The drawing of the high-efficiency AC-to-DC SEPIC circuit is presented in Fig. 3. This circuit is called high efficiency SEPIC circuit due to its efficiency of over 99%. The circuit includes four inductors (L_1, L_2, L_3, and L_4), two capacitors (C_1, C_2), diodes, and an electronic switch (M_1). Since the source voltage applied to the circuit is of AC type, the conversion on both positive and negative half cycles of this voltage is necessary. The inductors, L_1, L_2, and the capacitor, C_1 work in the positive half cycle, and the inductors, L_3, L_4, and the capacitor, C_2 work in the negative half cycle of the supply voltage. The inductors L_+, L_-, and capacitors C_+, C_- act as the input side filtering circuit. C_L and R_L act as the load capacitor and load resistance respectively [33].

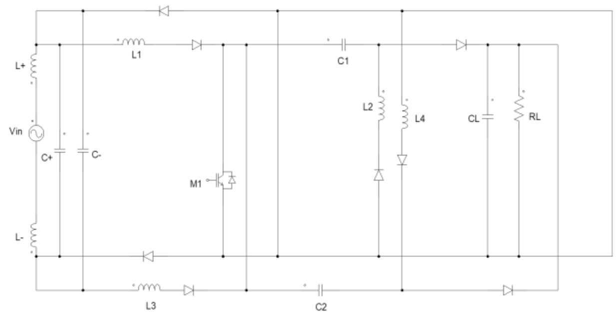

Fig. 3. High-efficiency AC-to-DC SEPIC circuit [33]

Circuit parameters and their values used in this circuit are as follows:

The peak source voltage (V_{in}) applied to the circuit is 300 V with a frequency of 50 Hz. An IGBT has been employed as a switching device. The inductances of different inductors L_1, L_2, L_3, and L_4 were set at 2 mH each. The filter circuit contains two inductors, L_+ and L_- whose inductances were set at 2.5 mH each, and the capacitance of the capacitors C_1 and C_2 were set at 1 µF each. The capacitances of the filter circuit capacitors C_+ and C_- were given as 2 µF each. The capacitance of the output side capacitor, C_L was given a magnitude of 20 µF, and the resistance of the load resistor, R_L was set at 100 Ω. The circuit operates in the inner loops in the positive half cycle and the outer loops in the negative half cycle [33].

D. Input Switched AC-to-DC SEPIC Circuit

The drawing of the input switched AC-to-DC SEPIC circuit is depicted in Fig. 4. The circuit includes three inductors (L_1, L_2, and L_3), four capacitors (C_1, C_2, C_{o1}, and C_{o2}), six diodes (D_1-D_6), and a switch (S). A resistor, R_o is utilized as the load or output resistor of the circuit [34].

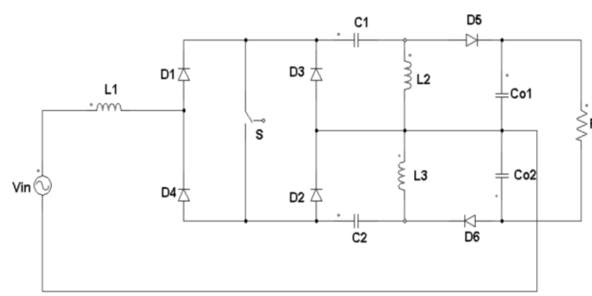

Fig. 4. Input switched AC-to-DC SEPIC circuit [34]

Circuit parameters and their values used in this circuit are as follows:

The peak source voltage (V_{in}) applied to the circuit is 300 V with a frequency of 50 Hz. An IGBT has been employed as a switching device. The inductance values of the inductors L_1, L_2, and L_3 are 10 mH, 12 mH, and 12 mH respectively when the converter functioned as a buck converter and those are 6 mH, 5 mH, and 5 mH when the circuit is operated as a boost converter. However, the capacitance values of the capacitors C_{o1} and C_{o2} are 330 μF each and those of C_1 and C_2 are 1.5 μF each with the resistance of the load resistor, R_o of 100 Ω when the converter is operated as both buck and boost converters [34].

E. Improved Performance AC-to-DC SEPIC Circuit

The circuit diagram of improved performance AC-to-DC SEPIC configuration is presented in Fig. 5. The circuit includes four inductors (L_1, L_2, L_3, and L_4), five capacitors (C_{o1}, C_{o2}, C_1, C_2, and C_o), six diodes (D_1-D_6), and a switch (S). A resistor R_L is used as the load of the circuit [35].

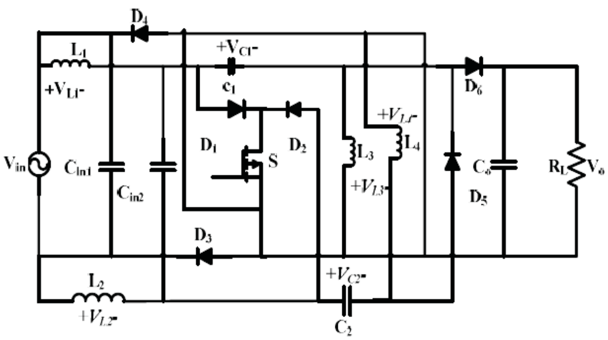

Fig. 5. Improved performance AC-to-DC SEPIC circuit [35]

Circuit parameters and their values used in this circuit are as follows:

The peak source voltage (V_{in}) applied to the circuit is 300 V with an operating frequency value of 50 Hz. An IGBT device has been utilized as an exchanging device. The inductance values of the inductors L_1 and L_2 are 2.8 mH each and those of the inductors L_3 and L_4 are 1.8 mH each. The capacitance values of the input capacitors C_{in1} and C_{in2} are 5.5 μF each, those of capacitors C_1 and C_2 are of 0.8 μF each, and that of output capacitor, C_o is of 220 μF with the resistance of the load resistor, R_L of 100 Ω [35]

III. RESULTS AND DISCUSSIONS

In this work, five various configurations of single-phase single-switch AC-to-DC SEPIC topologies were explored in an open-loop using the PSIM software version 9.1.1. Table I furnishes the comparative data of different topologies of the SEPIC Configuration (SC). Based on this investigation on five different SEPIC topologies, a performance appraisal was made in terms of efficiency, power factor of the input line current, Total Harmonic Distortion (THD) [36], and the output voltage gain by altering two parameters, viz. duty cycle, and the load.

TABLE I
COMPARING THE VARIOUS TOPOLOGIES OF THE AC-TO-DC SEPIC CIRCUIT

Topology	Figure #	Ref. #	Switch/ Capacitor Number	Diode/ Inductor Number
Switched Capacitor SC	1	31	1/5	8/3
Modified SC	2	32	1/4	5/4
High-efficiency SC	3	33	1/5	8/6
Input Switched SC	4	34	1/4	6/3
Improved Performance SC	5	35	1/5	6/4

A. Performance evaluation with duty cycle change

At first, the open-loop analysis of five topologies of AC-to-DC SEPIC circuits was performed by changing the duty cycle from 10% to 90%. The simulated results of the four performance parameters are furnished in Table II with the increment of the duty cycle values. The load resistance in all circuits was fixed at 100 Ω and the switching frequency was set to 10 kHz. After that, all the four parameters were plotted against the duty cycle values for all the five topologies in one figure each in Figs. 6-9. The figure demonstrates that the efficiency is better in the high-efficiency SEPIC circuit and the lowest efficiency is shown by the modified SEPIC circuit as in Fig. 6. On the other hand, the high-efficiency and modified SEPIC circuits show a better power factor and the switched capacitor SEPIC circuit shows the worst power factor as in Fig. 7. The switched capacitor SEPIC circuit performs much better at all duty cycles when THDs are taken into consideration as in Fig. 8. Conversely, the better voltage gain is given by both inputs switched and improved performance SEPIC circuits at higher duty cycles as shown in Fig. 9.

TABLE II
PERFORMANCE EVALUATION OF VARIOUS TOPOLOGIES OF SINGLE-PHASE SINGLE-SWITCH NON-ISOLATED AC-TO-DC SEPIC CIRCUIT WITH DUTY CYCLE CHANGE

Duty Cycle	Topology	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
	Switched Capacitor SC	95.03	0.22	1.91	0.65
	Modified SC	82.43	0.94	19	0.22
0.1	High-efficiency SC	97.27	0.537	14.3	0.21
	Input Switched SC	98.62	0.88	49.45	0.27
	Improved Performance SC	95.72	0.28	26.84	0.32
	Switched Capacitor SC	97.93	0.67	2.52	1.25

Duty Cycle	Topology	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
	Modified SC	83.88	0.96	9.50	0.44
0.2	High-efficiency SC	99.25	0.877	8.97	0.38
	Input Switched SC	98.92	0.90	41.03	0.60
	Improved Performance SC	97.97	0.66	43.63	0.61
	Switched Capacitor SC	98.68	0.97	0.33	1.76
	Modified SC	88.10	0.96	6.90	0.75
0.3	High-efficiency SC	99.49	0.961	6.066	0.54
	Input Switched SC	99	0.86	56.33	1.11
	Improved Performance SC	98.41	0.85	38.55	0.91
	Switched Capacitor SC	98.55	0.95	0.79	2.10
	Modified SC	92.20	0.97	5.80	0.95
0.4	High-efficiency SC	99.57	0.977	7.94	0.70
	Input Switched SC	98.98	0.87	53.19	1.71
	Improved Performance SC	98.52	0.92	29.00	1.24
	Switched Capacitor SC	98.31	0.72	0.21	2.09
	Modified SC	93.33	0.98	4.90	1.33
0.5	High-efficiency SC	99.63	0.97	14.03	0.93
	Input Switched SC	98.91	0.88	45.98	2.49
	Improved Performance SC	98.57	0.95	21.78	1.58
	Switched Capacitor SC	97.89	0.48	0.33	1.82

Duty Cycle	Topology	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
	Modified SC	94.10	0.99	5	1.52
0.6	High-efficiency SC	99.66	0.969	18.45	1.30
	Input Switched SC	98.80	0.88	34.76	3.41
	Improved Performance SC	98.59	0.95	26.61	2.16
	Switched Capacitor SC	97.34	0.33	0.42	1.53
	Modified SC	93.80	0.98	14.98	2.10
0.7	High-efficiency SC	99.61	0.973	22.8	1.90
	Input Switched SC	98.63	0.83	20.41	4.41
	Improved Performance SC	98.52	0.90	39.53	3.19
	Switched Capacitor SC	96.60	0.20	0.60	1.21
	Modified SC	91.90	0.96	11.88	2.90
0.8	High-efficiency SC	99.01	0.944	17.88	2.99
	Input Switched SC	98.16	0.64	7.246	5.15
	Improved Performance SC	98.30	0.84	35.02	4.75
	Switched Capacitor SC	91.76	0.10	0.39	0.63
	Modified SC	93.40	0.93	14.32	3.45
0.9	High-efficiency SC	92.77	0.486	3.72	3.13
	Input Switched SC	95.48	0.20	1.44	3.21
	Improved Performance SC	97.58	0.72	34.37	6.98

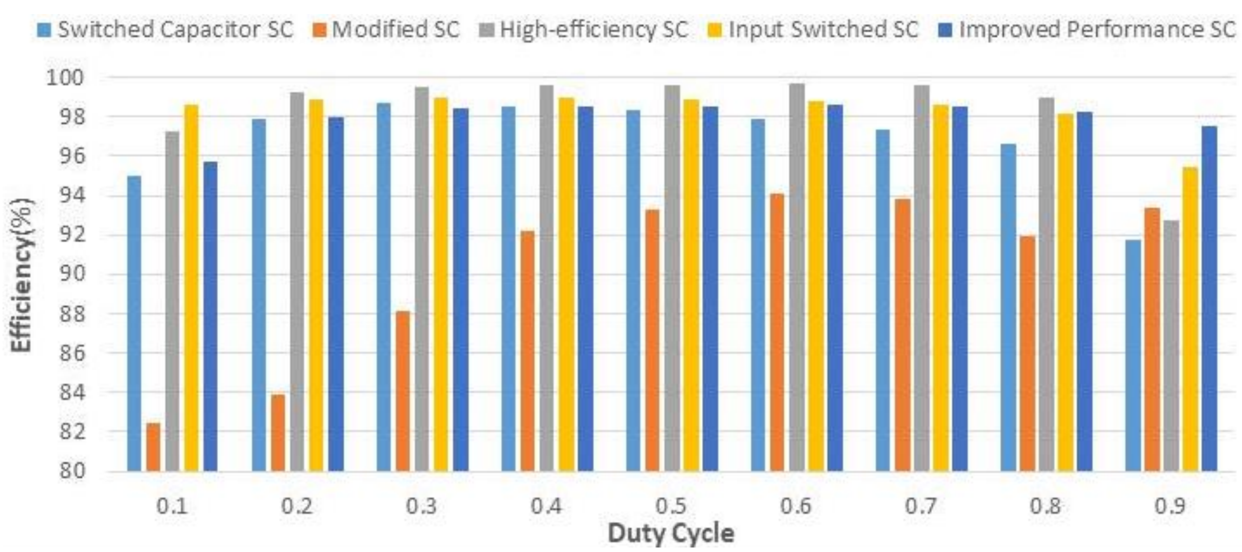

Fig. 6. Comparison of efficiency among various topologies of single-phase single-switch non-isolated AC-to-DC SEPIC circuits with duty cycle change

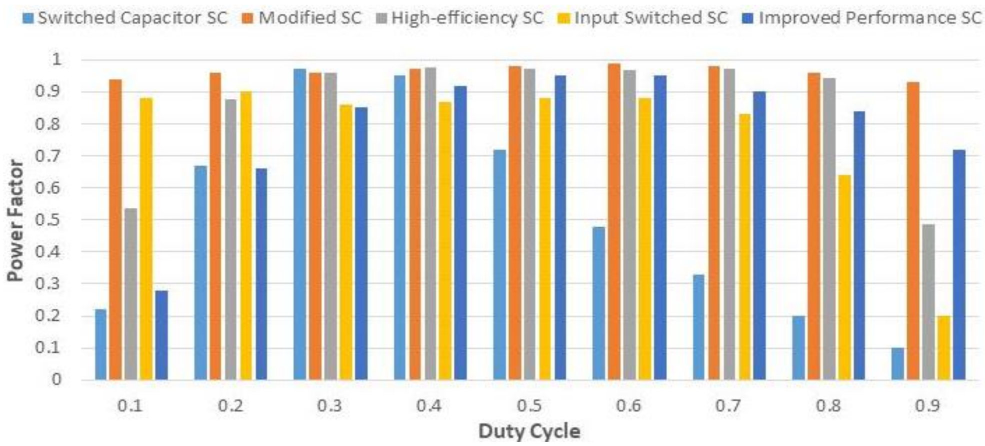

Fig. 7. Comparison of power factor among various topologies of single-phase single-switch non-isolated AC-to-DC SEPIC circuits with duty cycle change

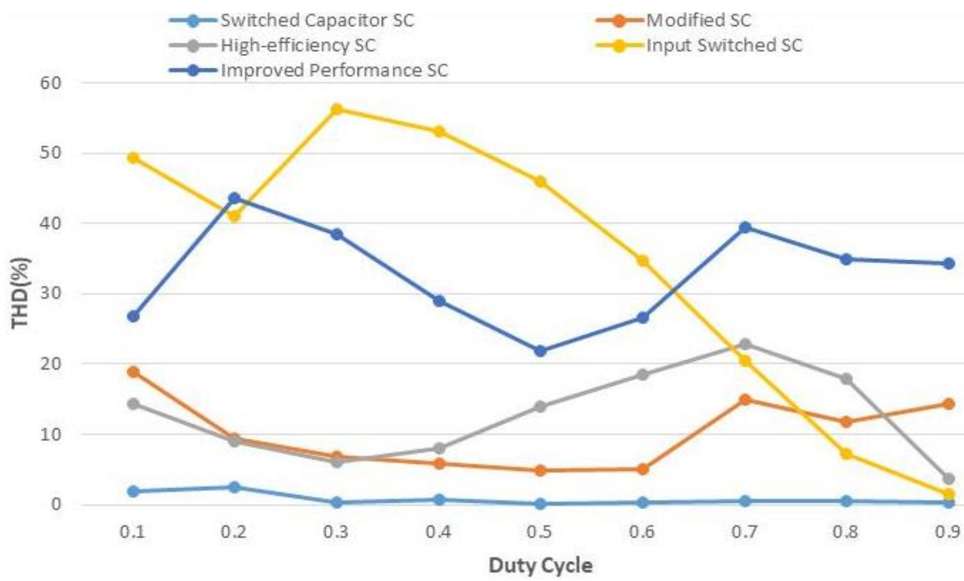

Fig. 8. Comparison of THD among various topologies of single-phase single-switch non-isolated AC-to-DC SEPIC circuits with duty cycle change

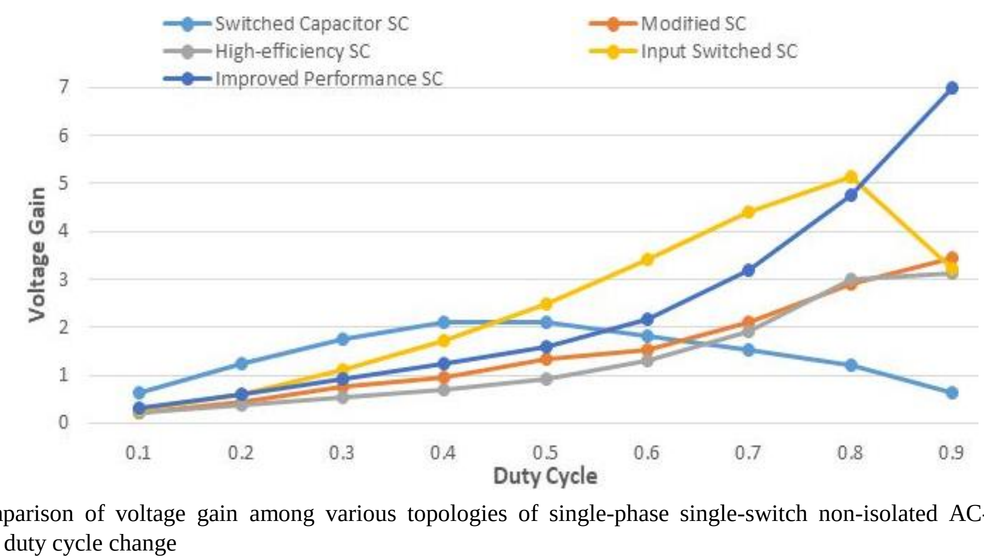

Fig. 9. Comparison of voltage gain among various topologies of single-phase single-switch non-isolated AC-to-DC SEPIC circuits with duty cycle change

B. Performance evaluation with load change

At first, the open-loop analysis of five topologies of AC-TO-DC SEPIC circuits was performed by changing the load from 50 Ω to 500 Ω. The simulated results of the four performance parameters are furnished in Table III with the increment of the load resistance values. The duty cycle in all circuits was fixed at 60% and the switching frequency was set to 10 kHz. After that, all the four parameters were plotted against the load resistance values for all the five topologies in one figure each in Figs. 10-13. The figure demonstrates that the efficiency is better in the high-efficiency SEPIC circuit and the lowest efficiency is shown by the modified SEPIC circuit at a wide range of the load resistance values as in Fig. 10. On the other hand, two SEPIC circuits, such as high-efficiency and modified circuits demonstrate the highest Power Factors (PFs) and the switched capacitor circuit demonstrates the worst power factor as shown in Fig. 11 for all ranges of the load resistances used in the simulation environment. However, the switched capacitor SEPIC circuit performs much better at all loads when THDs are taken into consideration as in Fig. 12. Conversely, the better voltage gain is provided by the improved performance and switched capacitor SEPIC circuits at higher load resistance values and the input switched SEPIC circuit demonstrates almost constant voltage gain for a wide range of load resistance values as in Fig. 13.

TABLE III
PERFORMANCE VARIATION ON DIFFERENT TOPOLOGIES OF SINGLE-PHASE SINGLE-SWITCH NON-ISOLATED AC-TO-DC SEPIC CIRCUIT WITH LOAD RESISTANCE CHANGE

Load (Ω)	Topology	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
	Switched Capacitor SC	98.26	0.52	0.17	1.26
	Modified SC	94.87	0.99	4.7	1.08
50	High-efficiency SC	99.78	0.989	12.26	1.10
	Input Switched SC	99.18	0.96	18.95	2.74
	Improved Performance SC	99.19	0.90	46.34	2.06
	Switched Capacitor SC	97.89	0.48	0.33	1.82
	Modified SC	94.10	0.99	5	1.52
100	High-efficiency SC	99.66	0.969	18.45	1.30
	Input Switched SC	98.80	0.88	34.76	3.41
	Improved Performance SC	98.59	0.95	26.61	2.16
	Switched Capacitor SC	97.59	0.48	0.072	2.25
	Modified SC	93.80	0.99	5.08	1.88
150	High-efficiency SC	99.59	0.946	26.39	1.99
	Input Switched SC	98.46	0.85	41.50	3.52
	Improved Performance SC	97.96	0.95	17.33	2.38
	Switched Capacitor SC	97.30	0.48	0.045	2.60
	Modified SC	94.20	0.99	4.85	2.18
200	High-efficiency SC	99.48	0.932	31.51	2.17
	Input Switched SC	98.10	0.83	45.88	3.58
	Improved Performance SC	97.33	0.95	17.80	2.73
	Switched Capacitor SC	97.00	0.48	0.077	2.91
	Modified SC	94.32	0.99	5.10	2.33
250	High-efficiency SC	99.36	0.932	33.02	2.34
	Input Switched SC	97.73	0.82	48.93	3.63
	Improved Performance SC	96.71	0.95	18.07	3.04
	Switched Capacitor SC	96.69	0.48	0.099	3.19
	Modified SC	93.88	0.99	5.22	2.70
300	High-efficiency SC	99.25	0.938	32.28	2.49
	Input Switched SC	97.35	0.81	51.30	3.68
	Improved Performance SC	96.08	0.95	18.24	3.32
	Switched Capacitor SC	96.37	0.48	0.11	3.44
	Modified SC	93.21	0.99	4.90	3.10
350	High-efficiency SC	99.13	0.946	30.32	2.60
	Input Switched SC	96.98	0.80	52.97	3.72
	Improved Performance SC	95.46	0.95	18.36	3.57
	Switched Capacitor SC	96.06	0.48	0.12	3.67
	Modified SC	93.10	0.99	5.12	3.40
400	High-efficiency SC	99	0.955	27.63	2.70
	Input Switched SC	96.61	0.79	54.33	3.75
	Improved Performance SC	94.85	0.95	18.44	3.80
	Switched Capacitor SC	95.75	0.48	0.12	3.89
	Modified SC	93.50	0.99	5.14	3.77
450	High-efficiency SC	98.89	0.964	24.40	2.79
	Input Switched SC	96.24	0.77	55.32	3.78
	Improved Performance SC	94.23	0.95	18.51	4.02
	Switched Capacitor SC	95.43	0.48	0.13	4.09
	Modified SC	93.50	0.99	5.20	3.90
500	High-efficiency SC	98.77	0.972	20.64	2.86
	Input Switched SC	95.87	0.76	56.12	3.80
	Improved Performance SC	93.62	0.95	18.56	4.22

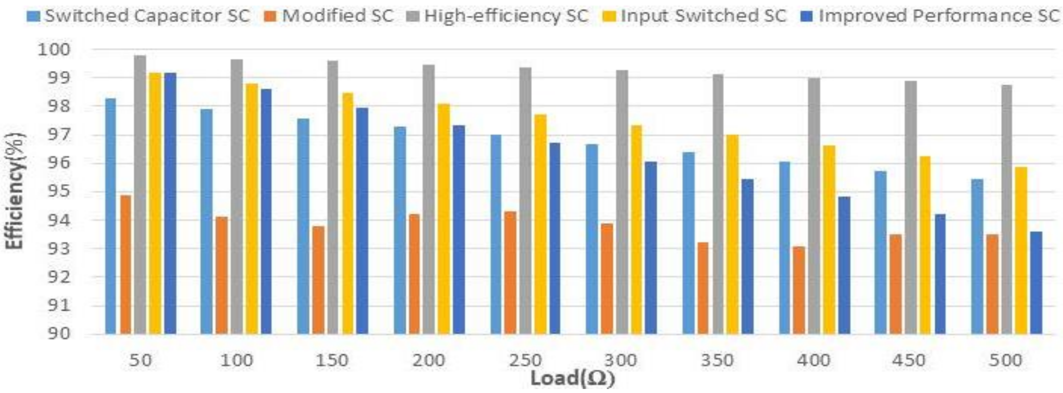

Fig. 10. Comparison of efficiency among various topologies of single-phase single-switch non-isolated AC-TO-DC SEPIC circuits with load change

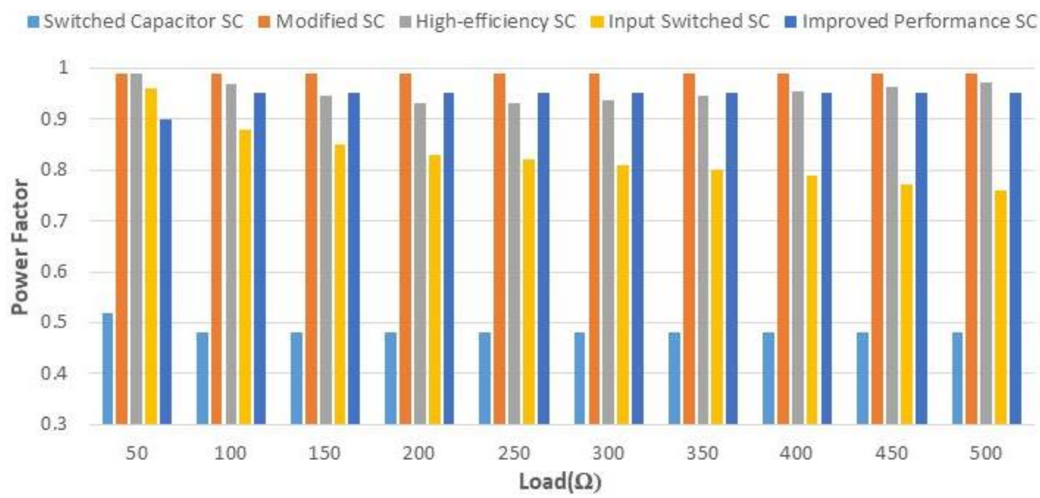

Fig. 11. Comparison of PFs among various single-phase single-switch non-isolated AC-to-DC SEPIC circuits with load change

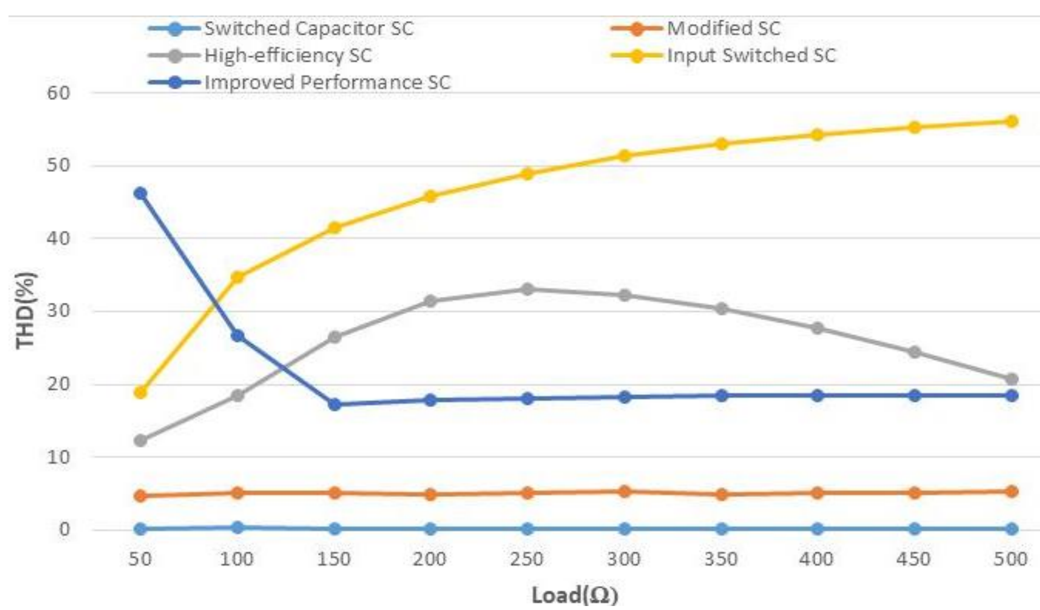

Fig. 12. Comparison of THDs among various single-phase single-switch non-isolated AC-to-DC SEPIC circuits with load change

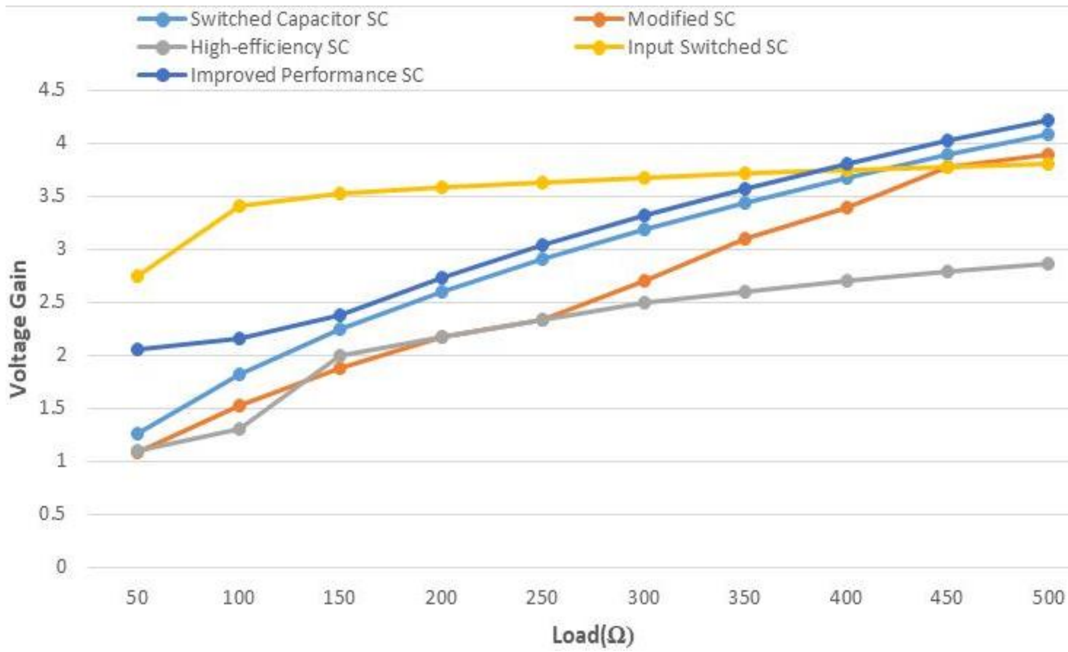

Fig. 13. Comparison of voltage gain among various topologies of single-phase single-switch non-isolated AC-to-DC SEPIC circuits with load change

IV. Conclusion

This comparative research paper provides an in-depth and open-loop analysis of five diverse configurations of single-phase, single-switch non-isolated AC-to-DC SEPIC circuits. To assess the performance and evaluate each converter topology, the duty cycle was increased from 10% to 100%, and the load resistance was increased from 50 Ω to 500 Ω. Simulations data were tabulated for each converter and plotted against the duty cycle and load. After a comparative study, it was found that both the input switched and improved performance SEPIC circuits at higher duty cycles demonstrate the better voltage gain and the input-switched converter shows higher THDs at higher load resistances. The efficiency of a high-efficiency SEPIC circuit is better (over 99%) than that of the other SEPIC circuit for a wide range of duty cycle or load resistance deviation. This type of comparison helps the circuit designers to select the optimum SEPIC topology in power electronic circuit design and real-time applications.

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